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Determination of energy barrier profiles for high-*k* dielectric materials utilizing bias-dependent internal photoemission

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We utilize bias-dependent internal photoemission spectroscopy to determine the metal/dielectric/silicon energy barrier profiles for $Au/HfO_2/Si$ and $Au/Al_2O_3/Si$ structures. The results indicate that the applied voltage plays a large role in determining the effective barrier height and we attribute much of the variation in this case to image potential barrier lowering in measurements of single layers. By measuring current at both positive and negative voltages, we are able to measure the band offsets from Si and also to determine the flatband voltage and the barrier asymmetry at 0 V. Our SiO_2 calibration sample yielded a conduction band offset value of 3.03 ± 0.1 eV. Measurements on HfO_2 give a conduction band offset value of 2.7 ± 0.2 eV (at 1.0 V) and Al_2O_3 gives an offset of 3.3 ± 0.1 (at 1.0 V). We believe that interfacial SiO_2 layers may dominate the electron transport from silicon for these films. The Au/HfO_2 barrier height was found to be 3.6 ± 0.1 eV while the Au/Al_2O_3 barrier is 3.5 ± 0.1 eV. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1812831]

The study of high-*k* dielectrics as a replacement for SiO_2 in complementary metal-oxide-semiconductor devices has become a field of enormous interest.[1–3] In this letter, we investigate the band-offset characteristics of high-*k* dielectrics on silicon. We utilize internal photoemission spectroscopy, a simple optical method developed in the 1960s,[4,5] which has seen recent renewed interest in order to gain information about barrier heights, trap states and interface dipoles in high-*k* dielectrics.[6] In this technique, a bias is applied across a dielectric structure, while tunable monochromatic light shines on the sample. At a threshold photon energy, electrons from the substrate (or metal gate) are excited by internal photoemission over the dielectric barrier.[7] This threshold energy corresponds to the barrier height of the dielectric. Using bias-dependent internal photoemission spectroscopy, we have determined a barrier height profile as a function of voltage. By measuring the barrier height at both positive and negative voltages, band offsets with respect to silicon (and also the metal gate) can be determined in addition to the flatband voltage and barrier asymmetry at 0 V.

In our experimental system, we utilize a 1000 W Hg–Xe lamp with a monochromator as our light source. We use a voltage source/femtoammeter to apply the bias across the sample and to measure the current at each bias. The system is computer controlled by LabView so that the light can be scanned between 1 and 6 eV at any bias and photon energy step size. A multifunction optical meter is used to determine the lamp output spectrum to normalize the photoemission yield. Fused silica lenses are used to focus the light onto the top gold contact of the sample, which is held vertically.

The dielectric samples are grown on degenerately phosphorous doped *n*-type silicon to minimize the voltage drop across the depletion region in the silicon, and enhance the accuracy of our measurement. The dielectrics presented in this letter are HfO_2 and Al_2O_3 grown by atomic layer deposition.[8,9] Before deposition, samples were dipped in a 5% HF solution for 30 s followed by a 3 min UV/ozone cleaning. Al_2O_3 films were grown using de-ionized water (DI H_2O) and trimethylaluminum ($Al[CH_3]_3$), while HfO_2 films were grown using DI H_2O and tetrakis(diethylamido)hafnium ($Hf[NEt_2]_4$). Nitrogen was used as the carrier gas, and the deposition temperature was 225 °C. The top electrode is a 12 nm layer of evaporated gold, which is sufficiently transparent so that the light source can photoexcite carriers in the silicon. The back contact is indium.

As a calibration for our experimental system, we analyzed a 15 nm thermally grown SiO_2 film deposited an *n*-Si (1–10 Ω cm doping). The photocurrent was measured as the photon energy was scanned at many voltages between −10 and 10 V. Figure 1 shows the raw photocurrent versus photon energy spectra for a variety of voltages (from −0.5 to +3.0 V). It is evident from these plots that the sign of the photocurrent depends strongly on the applied voltage, and the peaks in photocurrent correspond with the peaks in Hg–Xe lamp output (see Fig. 1 inset). For voltages from −10 V up to +0.7 V, negative currents were observed. At +0.7 V, the photocurrent switched signs and was positive for all higher positive voltages. We suggest that for positive photocurrents, collected electrons originate in the silicon, while the negative photocurrents indicate that electrons are mainly being generated in the metal gate contact. We determined

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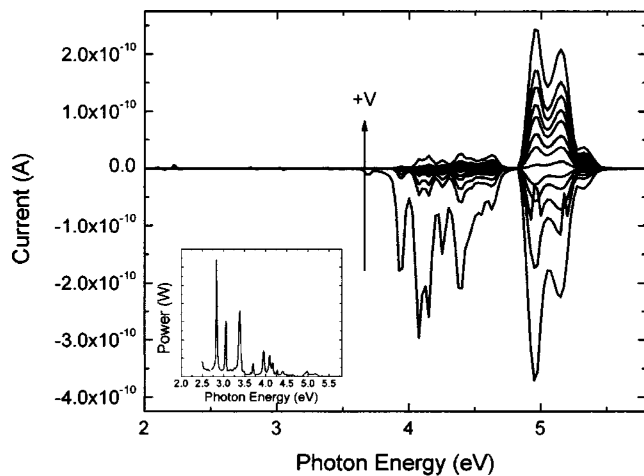

FIG. 1. Current through 15 nm SiO_2 film as a function of incident photon energy. Inset: output spectrum of Hg–Xe light source.

0.7 V to be the voltage where the currents from the metal matched those coming from the semiconductor. We expect this voltage to be close to flatband for single dielectric layers.

The next analysis step is to calculate the photocurrent yield

$$Y = \frac{I \cdot \hbar\omega}{P}, \tag{1}$$

where I is measured current in amperes, P is the absorbed light power in watts, $\hbar\omega$ is the photon energy in eV, and Y is the yield in electrons/photon. Each individual current versus photon energy curve is divided by the incident photon energy spectrum. The square root, cube root, or 2/5 power of the yield is then plotted versus photon energy as is shown in Fig. 2 for the 15 nm SiO_2 sample. The x intercept is then extracted and is reported as the band offset relative to the valence band of silicon. We assume that most electrons are emitted from the valence band since the number of filled initial states is much higher than in the conduction band. The literature is in general agreement that the square root is the appropriate power for intercept extraction when considering electrons emitted from a metal.[10,11] The case where electrons are emitted from the semiconductor is not well resolved. Semiclassical calculations suggest that taking a 2/5 power of the yield is correct[12] and a quantum mechanical correction to the theory predicts that the cube root is correct[13] when analyzing photocurrent from the valence band of a semiconductor.[14] In order to most thoroughly report the relevant results, we have computed offsets based on models assuming both the 2/5 power and the cube root of the yield for these situations.[15]

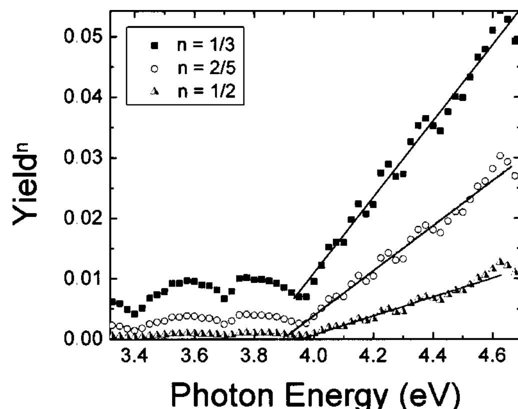

FIG. 2. Yield to the 1/3, 2/5, and 1/2 power. A linear fit to these curves is extrapolated to the x axis to provide a numerical value for the barrier height.

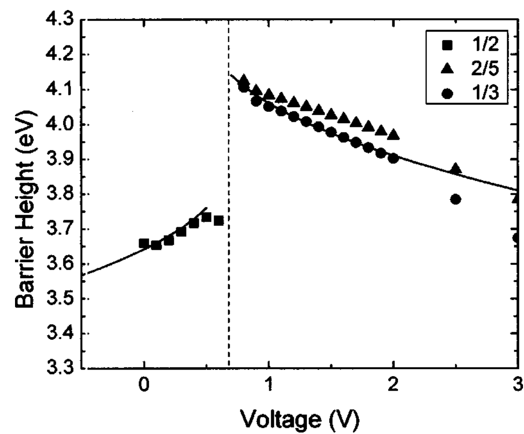

FIG. 3. Barrier height profile as function of voltage for 15 nm SiO_2 on n-Si. The dotted line indicates the voltage at which the current switches sign. The square dots on the left of the dotted line are extracted from the yield$^{1/2}$ curves and indicate the barrier for electrons from the metal. The triangles on the right are the barrier heights extracted from the yield$^{2/5}$ curves. The circles on the right are from the yield$^{1/3}$ curves. The triangles and circles indicate the barrier for electrons coming from the silicon substrate. This simulation takes into account image potential barrier lowering.

After extracting band offsets for each voltage, we obtain a barrier height profile as a function of voltage, as can be seen in Fig. 3 for 15 nm SiO_2. The points on the left of the vertical dotted line are for electrons emitted from the metal, the points on the right are for electrons emitted from the semiconductor. As can be seen, the band offset varies greatly with applied voltage, and this illustrates that it is of the utmost importance to report a corresponding bias voltage associated with a measured band offset. We report our band offsets as the point nearest to flat band, where electrons are coming from the semiconductor, or in the case of our SiO_2 film, 4.13 ± 0.1 eV. When we subtract the 1.1 eV SiO_2 band gap, we find that the Si/SiO_2 conduction band offset is 3.03 ± 0.1 eV. Ultimately, our results for SiO_2 fit well to what is expected for SiO_2 films with image potential barrier lowering.[11] The image potential barrier lowering simulations are shown by the black lines and can be represented by the equation (in energy units)

$$V_i = -1.15\lambda s^2/x(s-x), \tag{2}$$

where

$$\lambda = e^2 \ln 2/8\pi\varepsilon s, \tag{3}$$

e is the electron charge, and s and ε are the thickness and dielectric constant of the insulating layer. The distance of the electron from the first (source) electrode is x. The method for approximating image barrier lowering is described in Ref. 16. The image force was approximated as that of an insulator between two metallic electrodes. In general, the silicon substrates used in our experiments are highly doped, so this is a reasonable approximation although the thin depletion layer in the Si will somewhat modify the result. For SiO_2, we assumed an optical dielectric constant of 2.5.

Similar analyses were completed for Al_2O_3 and HfO_2 films on n-Si ($0.0001\ \Omega$ cm). The resulting barrier height

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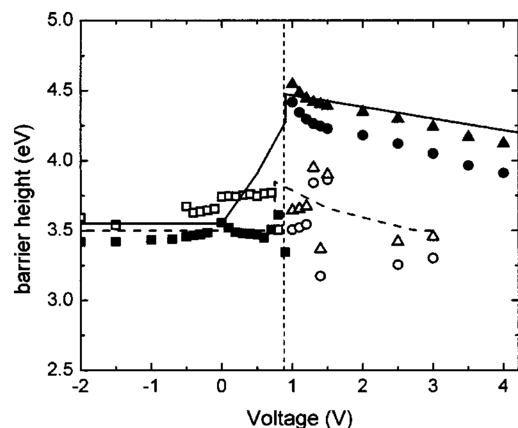

FIG. 4. Barrier height profile for HfO_2 and Al_2O_3 on n^+-Si. The data and barrier height simulation curves on the left hand side of the vertical dashed line represent negative photocurrents. The data and simulation curves on the right hand side represent positive photocurrents. The open symbols and dashed lines are for HfO_2 while the solid symbols and solid lines are for Al_2O_3. Squares indicate data extracted from yield$^{1/2}$ vs energy curves. Triangles correspond to yield$^{2/5}$ data while circles correspond to yield$^{1/3}$ data. This simulation considers the maximum barrier height at each voltage and the depletion region in the silicon substrate.

profiles and barrier height simulations are shown in Fig. 4. The barrier height profiles for these two materials are not nearly as clear as for SiO_2. This is particularly true for HfO_2—a result of leakage through the barrier and greater difficulty in extracting band offsets from the yield curves. Transmission electron microscopy analysis revealed that interfacial SiO_2 layers 2.2 nm thick were present between the HfO_2 and Al_2O_3 dielectric and semiconductor. These interfacial layers could be attributed to the UV/ozone clean during the substrate preparation or a postdeposition 600 °C anneal in Ar+2000 ppm O_2, and could account for the higher measured band offsets compared with literature values, though the electrical characteristics of these layers are unknown.

Because of the presence of interfacial layers in the Al_2O_3 and HfO_2 samples, the analysis for these films is slightly more complicated than for SiO_2. The measured barrier height (from the Si valence band) for 16.1 nm Al_2O_3 is 4.6±0.1 eV (at 1.0 V). After subtracting the Si band gap (1.1 eV), the Al_2O_3 conduction band offset is found to be 3.5±0.1 eV (at 1.0 V), but this probably corresponds most directly to the interfacial layer than to the Al_2O_3 layer itself. For this reason, another quantity of interest is the Au/Al_2O_3 barrier, which is observed to be 3.5±0.1 eV. There is a discontinuity at the point at which the originating carrier electrode changes from the metal to the silicon (at the vertical dotted line). Using a consistent set of parameters (Al_2O_3 $\kappa=9$, SiO_x $\kappa=3.9$), this asymmetry can be understood to first order if we consider the charge that is generated in the metal compared with those originating in the silicon for the $Au/Al_2O_3/SiO_x/Si$ barrier. The results for this simulation (accounting for Si depletion) are shown by the solid line in Fig. 4. The absence of the slope between 0 and 0.9 V is not well understood, but the fact that we can simulate the general shape of the profile and accurately approximate the barrier heights for electrons coming from each electrode is very encouraging. The experimental literature reports conduction band offsets of 2.78 and 2.15 eV for Al_2O_3, while theoretical calculations predict 2.8 eV.[6,17]

Similar analysis can be done for HfO_2 (open symbols in Fig. 4), but because of the degraded data quality attributed to leakage from the substrate, it is more difficult to verify our data by simulation. The dashed curve indicates a barrier lowering simulation for the HfO_2 barrier (HfO_2 $\kappa=22$, SiO_x $\kappa=3.9$). The data quality is good when the electrons originate from the metal (from −0.5 to 0.9 eV) and we can determine a Au/HfO_2 barrier height of 3.6±0.1 eV. Using the same reasoning as for Al_2O_3, based on our data, our best approximation for the Si/HfO_2 barrier height (from valence band) is 3.8 eV±0.2 eV. This corresponds to a conduction band offset with respect to Si of 2.7±0.2 eV. The experimental literature reports conduction band offsets of 2.0 and ~1.2 eV for HfO_2, while theoretical calculations predict 1.5 eV.[18–20] Further effects of barrier lowering in HfO_2/Al_2O_3 heterostructures will be addressed in a paper to be published soon (see Ref. 21 for background).

The high-κ field has been plagued by the growth of unwanted interfacial layers at the dielectric/silicon interface. Progress is being made to decrease these layers by careful cleaning and passivation of the silicon surface before growth, but eliminating these layers completely remains a great challenge.[22] Although interfacial layers will in general modify the measurements, by careful use of our barrier profile technique, and by selecting the barrier height at specific voltages (and thus specific band alignment) we can gain a very good estimate of the band offset of any barrier. We have shown that profiling the barrier heights of dielectrics on silicon as a function of applied bias is a very viable and valuable technique for determining the effective band offset at any particular voltage.

[1] J. Kwo, M. Hong, B. Busch, D. A. Muller, Y. J. Chabal, A. R. Kortan, J. P. Mannaerts, B. Yang, P. Ye, H. Gossmann, A. M. Sergent, K. K. Ng, J. Bude, W. H. Schulte, E. Garfunkel, and T. Gustafsson, J. Cryst. Growth **251**, 645 (2003).
[2] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[3] H. R. Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G. A. Brown, C. D. Young, P. M. Zeitzoff, J. Gutt, P. Lysaght, M. I. Gardner, and R. W. Murto, Microelectron. Eng. **69**, 152 (2003).
[4] R. J. Powell, J. Appl. Phys. **41**, 2424 (1970).
[5] E. O. Kane, Phys. Rev. **127**, 131 (1962).
[6] V. V. Afanas'ev, M. Houssa, A. Stesmans, and M. M. Heyns, Appl. Phys. Lett. **78**, 3073 (2001).
[7] V. K. Adamchuk and V. V. Afanas'ev, Prog. Surf. Sci. **41**, 111 (1992).
[8] D. M. Hausmann, E. Kim, J. Becker, and R. G. Gordon, Chem. Mater. **14**, 4350 (2002).
[9] M. D. Groner, J. W. Elam, F. H. Fabreguette, and S. M. George, Thin Solid Films **413**, 186 (2002).
[10] R. H. Fowler, Phys. Rev. **38**, 45 (1931).
[11] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[12] E. O. Kane, Phys. Rev. **127**, 131 (1962).
[13] I.-S. Chen, T. N. Jackson, and C. R. Wronski, J. Appl. Phys. **79**, 8470 (1996).
[14] The cube root and 2/5 power laws do not apply to emission from the conduction band.
[15] V. V. Afanas'ev, M. Houssa, A. Stesmans, and M. M. Heyns, J. Appl. Phys. **91**, 3079 (2002).
[16] J. G. Simmons, J. Appl. Phys. **34**, 1793 (1963).
[17] R. Ludeke, M. T. Cuberes, and E. Cartier, Appl. Phys. Lett. **76**, 2886 (2000).
[18] V. V. Afanas'ev, A. Stesmans, F. Chen, X. Shi, and S. A. Campbell, Appl. Phys. Lett. **81**, 1053 (2002).
[19] S. Sayan, E. Garfunkel, and S. Suzer, Appl. Phys. Lett. **80**, 2135 (2002).
[20] J. Robertson, J. Vac. Sci. Technol. B **18**, 1785 (2000).
[21] J. D. Casperson, L. D. Bell, and H. A. Atwater, J. Appl. Phys. **92**, 261 (2002).
[22] K. Choi, H. Harris, S. Gangopadhyay, and H. Temkin, J. Vac. Sci. Technol. A **21**, 718 (2003).

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