JOURNAL OF APPLIED PHYSICS VOLUME 92, NUMBER 1 1 JULY 2002

Materials issues for layered tunnel barrier structures

Julie D. Casperson[a)]
Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, California 91125

L. Douglas Bell
Jet Propulsion Laboratory, Pasadena, California 91109

Harry A. Atwater
Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology, Pasadena, California 91125

(Received 8 October 2001; accepted for publication 28 March 2002)

Layered dielectric tunnel barriers are expected to greatly increase the program/erase speeds of nonvolatile floating gate memory devices and could allow both nanosecond program/erase times as well as archival data storage. We have correlated dielectric constants and band offsets with respect to silicon in order to help identify possible materials from which to construct these devices. A numerical model has been developed to assess potential layered tunnel barrier materials and structures suitable for integration into silicon electronics. With this model, we explore the relative dominance of Fowler–Nordheim tunneling and thermionic emission and we present simulated *I–V* curves for some candidate materials. © *2002 American Institute of Physics.*
[DOI: 10.1063/1.1479747]

I. INTRODUCTION

Currently, nonvolatile memory devices in applications such as cellular phones and digital cameras utilize floating gate field-effect transistor technology to store information. In such floating gate memories, charge is stored on a silicon floating gate that is separated from the substrate by a dielectric tunnel barrier as shown in Fig. 1.[1] This tunnel barrier controls the retention time and program/erase speed of the device. When a "program" bias is applied to the device, charge tunnels through the barrier and remains stored on the floating gate after the program voltage is removed. Typically, the tunnel barrier consists of a thin thermally-grown SiO_2 layer. In this geometry, the tunneling occurs through a triangular barrier [Fig. 1(a)] by Fowler–Nordheim tunneling. This type of tunneling results from the voltage applied to a homogeneous dielectric and it creates an effectively triangular barrier shape resulting from the bias. A conduction band diagram demonstrating Fowler–Nordheim tunneling is shown in Fig. 1(a).

Since the tunnel barrier must be able to inject a current during programming and to retain charge, a compromise must be made when designing memory devices that integrate a tunnel barrier. When the barrier is made relatively thick, long charge retention times are achieved, but a higher voltage (and a longer time) is required to program and erase the floating gate. When the barrier is thin, the program and erase process will be more rapid, but charge leakage will reduce the retention time. If a graded tunnel barrier could be constructed by appropriately varying the band offsets, an effective lowering of the barrier would be observed under an applied bias [See Fig. 1(b)]. This barrier lowering effect allows an increase in the tunnel current density and a subsequent increase in the floating gate program/erase speed.

As shown here by simulation, optimally graded structures would create a good balance between charge retention and program/erase speed. Such structures have been fabricated by epitaxy of $Al_xGa_{1-x}As/GaAs$ on GaAs, and they have been used to demonstrate charge injection through a barrier lowering effect, although the band offsets obtainable by this method could not lead to technologically interesting retention times at room temperature in AlGaAs/GaAs devices (<5 s at 273 K).[2] It has been suggested that a similar barrier lowering effect could be observed by approximating the graded barrier by layering dielectrics with varying band offsets onto silicon, although accurate simulation and appropriate silicon compatible materials systems have not been identified to date.[3–5] Our simulations show that three-layer structures provide a good approximation to the more optimal graded structure. In addition, these barriers provide band offsets that will result in good retention times and they could be readily integrated using current silicon technology. They could also be used in conjunction with other technologies such as nanocrystal floating gates to obtain truly archival data storage.[6] The symmetry property of the three-layer structures allows for increased speed for both the program and erase processes.

In the present paper, we perform a survey of silicon compatible dielectric materials and calculate the current–voltage (*I–V*) characteristics for some promising materials systems. Intensive research is currently being conducted on high dielectric constant materials such as Al_2O_3, Ta_2O_5, HfO_2, and $ZrSi_xO_y$ to potentially replace SiO_2 as the gate dielectric material for sub-0.1 μm complementary metal–oxide–semiconductor technology.[7] Because of this, the exploration of layered tunnel barriers is especially timely, and

a)Electronic mail: jcaspers@caltech.edu

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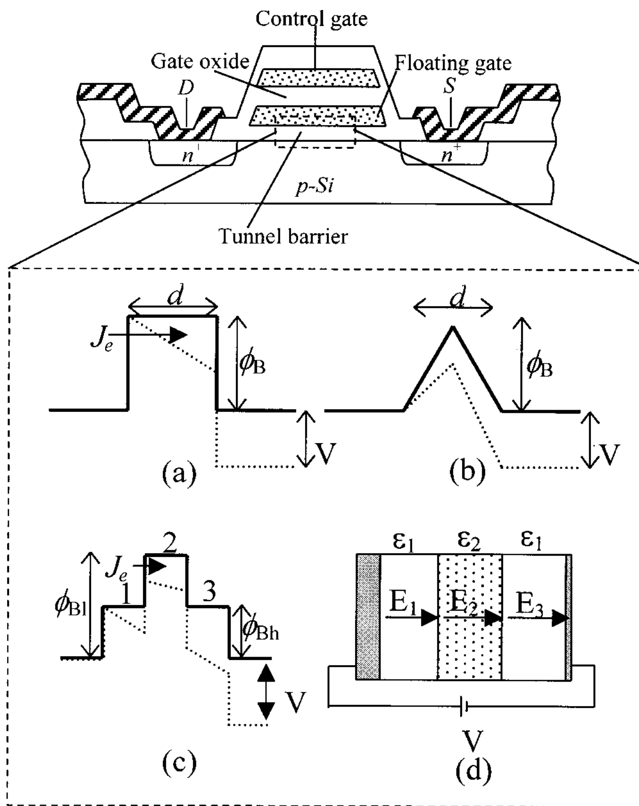

FIG. 1. Schematic representation of a floating gate memory. When a voltage is applied to the control gate and a bias is applied between the source (S) and drain (D), the channel opens to let a current flow. Some electrons also tunnel through the tunnel barrier and are stored on the silicon floating gate. The threshold voltage gives a measure of the amount of charge stored (after Ref. 1). Parts (a), (b), and (c) show conduction band edge diagrams of other types of tunnel barriers: (a) a typical uniform barrier; (b) idealized crested symmetric barrier; and (c) three-layer structure. Dotted lines show the barrier tilting caused by applied voltage V (after Ref. 3). Part (d) illustrates the three-layer capacitor structure that is referred to in (c). The left-hand electrode is silicon, the right-hand electrode is a metal contact, and dielectric constants ε, electric fields E, and applied voltage V are indicated. Through calculation, it is found that the amount of charge trapped in the triangular well that is formed at the interface of layer 1 and 2 is negligible.

knowledge obtained in this research will be useful in deciding upon appropriate materials for the layered barrier heterostructure fabrication approaches.

II. SIMULATION AND THEORY

Using a barrier transport model, we have calculated the I–V characteristics that would optimize the layered tunnel barrier structure. To correspond with a long retention time as well as a fast program/erase speed, the ideal I–V curves show a ratio of the current density at some maximum voltage $J_{\max}$ to the current density at some minimum voltage $J_{\min}$ to be at least as large as

$$\frac{J_{\max}}{J_{\min}(V=0)}=\frac{\tau_{\text{ret}}}{\tau_{\text{prog}}}=\frac{30\text{ yr}}{1\text{ ns}}\approx 10^{18}. \quad (1)$$

This value is based on an ideal retention time τ_{ret} for a device of at least 30 yr and a programming time τ_{prog} of at most 1 ns, yielding an overall current ratio of at least 10^{18}. This current ratio should occur between voltages of approximately 0 and 4 V to be compatible with current device technology. While it is important to obtain large current ratios, the absolute currents are also important because the nonvolatility and speed in data storage devices are affected by off-state and on-state currents, respectively. A reasonable off-state current for a gate of area 0.01 μm^2 would be 1 e/30 yr, or about 1.7×10^{-18} A/cm^2. The on-state current could be 100 e/ns or about 160 A/cm^2.

The tunneling current for any given bias is determined by the thermal distribution of electrons, Fermi functions, and the shape of the barrier. We have developed a barrier tunneling transport model to analyze possible barrier structures that incorporate the layered dielectrics on silicon with a metal contact. Because the dielectrics will be grown on silicon, our simulations include the effects of band bending due to the depletion region of the silicon. For this case, the values for band bending in a metal–semiconductor contact are used.[8] The model assumes the effective mass approximation and a plane-wave basis. The barrier layers and electrodes are treated as continuous media, which is a reasonable approximation for amorphous materials.[9] Tunneling current is calculated by numerically integrating over energy and carrier angle of incidence, and thus naturally includes the transport mechanisms of thermionic emission, Fowler–Nordheim tunneling, direct tunneling, and tunneling through the Schottky barrier of the silicon. The barrier transmission probability is calculated using numerical methods, which allows for analysis of resonant tunneling effects and localized charge densities trapped in potential minima. The current density includes the carrier transport (either electrons or holes) in both directions between the metal and semiconductor contact:

$$\begin{aligned} J&=J_{S-M}-J_{M-S}\\ &=\frac{4\pi m^* e}{h^3}\int\int \tau(\varepsilon,\theta)[f_s(\varepsilon)-f_m(\varepsilon)]\cos\theta\varepsilon d\varepsilon d\theta, \end{aligned} \quad (2)$$

where m^* is the electron effective mass in the semiconductor ($m^*=1$ is assumed in the metal), e is the electron charge, h is Planck's constant, and ε is the electron energy (in this equation only). The function $\tau(\varepsilon,\ \theta)$ is the single-electron transmission probability calculated for the entire potential structure, including the layered dielectrics and the silicon depletion region.[9] The variable θ is the solid angle of electron incidence on the barrier and f_s and f_m are the Fermi functions for the silicon substrate and metal contact, respectively.

The k-space integration in Eq. (2) can be done in a straightforward way by using numerical methods, with special care taken with the integration over energy. For certain barrier combinations, the transmission resonances can be extremely narrow, while at the same time having enough spectral weight to dominate the total current. The Wentzel–Kramers–Brillouin approximation is a well-known method for estimating tunneling through a barrier, but it is not useful in our case because it does not reproduce the described resonant transmission effects, nor does it properly treat the transmission near the band edges or through propagating states.[8]

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The numerical methods we use allow for the treatment of transmission that is dominated by such combined processes as thermionically-assisted tunneling.

By breaking the potential barrier into many exactly solvable square barriers, transmission can be calculated, within the independent-electron picture, to arbitrary precision. Essentially, this is a one-dimensional treatment, although parallel components of electron momentum are assumed. Those components are conserved since specular transmission is also assumed (no interface roughness or electron scattering).

In this model, values of effective mass and dielectric constant are assigned to each layer, and the potential structure is divided into a stack of thin square barriers. By matching the incoming and outgoing wavefunctions (ψ_1 and ψ_2) at each interface, using the matching conditions

$$\psi_1=\psi_2, \tag{3}$$

and

$$\frac{1}{m_1^*}\frac{d\psi_1}{dx}=\frac{1}{m_2^*}\frac{d\psi_2}{dx}, \tag{4}$$

we develop a recursion relation that involves only electron energy and the barrier heights and effective masses of adjacent slices. The final recursion relation yields the outgoing wave function amplitude and the transmission coefficient T through the entire structure:

$$T=(\nu_{\text{out}}/\nu_{\text{in}})|\Psi_{\text{out}}|^2, \tag{5}$$

giving the overall propagating solution. Here ν_{in} and ν_{out} are the electron velocities in the source and destination electrodes, respectively.

The recursion relations can be summarized as follows. The potential structure is divided into n layers. For each layer j, the recursion coefficients are given by

$$\alpha_j\equiv\left\{\frac{\frac{m_{j-1}\kappa_j}{m_j\kappa_{j-1}}f_{j-1}-1}{\frac{m_{j-1}\kappa_j}{m_j\kappa_{j-1}}f_{j-1}+1}\right\},$$

$$\beta_j\equiv\left\{\frac{f_{j-1}+1}{\frac{m_{j-1}\kappa_j}{m_j\kappa_{j-1}}f_{j-1}+1}\right\}\beta_{j-1}e^{-\kappa_{j-1}\Delta x}, \tag{6}$$

where

$$f_j\equiv\left[\frac{e^{\kappa_j\Delta x}+\alpha_j e^{-\kappa_j\Delta x}}{e^{\kappa_j\Delta x}-\alpha_j e^{-\kappa_j\Delta x}}\right],$$

and $\alpha_0=0$, $\beta_0=-1$. Here, Δx is the layer thickness, $\kappa_j=[2m_j/\hbar^2(V_j-E)]^{1/2}$ is the wave vector, and m_j is the effective mass. For layers in which the state is propagating, the wave vector is given instead by $\kappa_j=-i[2m_j/\hbar^2(E-V_j)]^{1/2}$. Thus each α_j or β_j coefficient for layer j depends on the coefficients for the previous $(j-1)$ layer. The final wave function amplitude for the outgoing state is given by

$$b_{n+1}=-\left\{\frac{f_n+1}{\frac{m_n\kappa_{\text{out}}}{m_{\text{out}}\kappa_n}f_n+1}\right\}\beta_n e^{-\kappa_n\Delta x}e^{-\kappa_{\text{out}}x_n}. \tag{7}$$

Once all the coefficients are obtained, wave function amplitudes can also be calculated at any point in the potential. These can be used for simple calculations of charge density σ:

$$\sigma=\frac{2e}{(2\pi)^3}\int\int|4(x)|^2 f_s(E)\,dx\,d^3k, \tag{8}$$

where the k-space and x integrations are taken over the extent of the potential well. By self-consistently solving the wave equation and Poisson's equation in the presence of a steady-state charge distribution, the effect of charging on the potential is also included. We use Eq. (8) to determine the amount of charge that builds up in the triangular well. In all cases presented here, charging effects, due to carrier accumulation in voltage-induced wells within the barrier structure, were negligible (less than a 10 mV change in the potential).

Because an effective mass model was used, reasonable values of mass were chosen for the electrodes and barrier materials. Electrode masses are much less important, only contributing to the prefactors in the expression for tunnel current. For metal electrodes, $m^*=1$ was used. For silicon, $m^*=0.2$ was used for electrons [the transverse mass for the conduction-band minimum at the center of the interface Brillouin zone for a (100)-oriented substrate].[8] Since all barrier materials were assumed to have zone-centered conduction-band minima, the other Si minima at large parallel wave vectors were assumed to contribute only weakly to total current. For the case of holes, an isotropic mass of 0.5 was used for the silicon substrate.[8] For the Al_2O_3 barrier layers, $m^*=0.5$ was used in the case of electrons; for Si_3N_4, 0.2 was used. Effective masses for holes were taken to be 0.5 for all barrier layers, and all barrier effective masses were assumed to be isotropic. Because total current is an integral over energy, and because the conduction and valence band effective masses are only appropriate for energies near the band edges, it is not straightforward to pick an appropriate value for simulations. Overall, however, we have chosen values that should give reasonable relative tunneling currents.[10]

Figures 1(c) and 1(d) show the device geometry for the three-layer structure under consideration. It consists of layered dielectric materials that are deposited on silicon and a metal contact on top of the dielectrics. By varying the barrier heights (compared to that of silicon) of the materials, the currents through the barrier are controlled, although the dielectric constants and thicknesses are the controllable parameters that directly affect the amount of barrier lowering. As can be shown using electrostatics,

$$E_1=\frac{V}{d_1+d_3+d_2(\varepsilon_1/\varepsilon_2)}, \tag{9}$$

where V is the applied voltage, E_1 is the electric field, d_i is the thickness, and ε_i is the dielectric constant in each region. The subscripts 1 and 3 refer to the low band offset layers on the outside of the structure, while the subscript 2 refers to the high band offset middle layer. [See Fig. 1(d)]. This relation indicates that to maximize the overall barrier lowering, the electric field through the first layer should be maximized. This means that the center barrier material should have a high dielectric constant and that the low band offset barrier

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TABLE I. Values for dielectric constant, band gap, conduction and valence band offsets for various dielectric materials.

Material	Dielectric constant	Band gap (eV)	CB offset from Si(eV)]	VB offset from Si(eV)
Al_2O_3	9[12]*	8.8[11]*	2.8[11]*	4.9[11]*
	8[13]	9[12]	2.78[12]	
$BaZrO_3$	43[14]*	5.3[11]*	0.8[11]*	3.4[11]*
CaO	12.0–12.2[14]*		7.5[15]*	
Gd_2O_3	14[16]	2.5[17]*	1.8[18]*	
HfO_2	40[19]*	6[11]*	1.5[11]*	3.4[11]*
	22[14]			
$HfSiO_x$	15–25[19]	6[11]		
	13[20]			
La_2O_3	20.8[14]	6[11]	2.3[11]	
MgO	9.8[14]	8.7[15]		
Sc_2O_3	13[14]	5.4[15]		
Si_3N_4	7.6[8]*	5.3[11]*	2.4[11]*	1.8[11]*
		5[21]		1.78[21]
SiO_2	3.9[8]*	9[11]*	3.5[11]*	4.4[11]*
Ta_2O_5	25[22]*	4.4[11]*	0.3[11]*	3[11]*
	23[13]			
TiO_2	80[13]*	3[15]	0[11]*	
	39[23]	3.27[24]*		
	80–110[7]	3.05[11]		
Y_2O_3	13–17[25]	5.5[15]*	1.3[11]*	3.6[11]*
	18[13]*	6[11]		
	11.3[14]	5.6[26]		
ZrO_2	25[19]*	5[15]*	1.4[11]*	3.3[11]*
	22[14]	5.8[11]		
$ZrSiO_x$	12.6[27]*	6[11]*	1.5[11]*	3.4[11]*

Notes: Values used in Fig. 2 are indicated by an asterisk. References are indicated by a superscript.

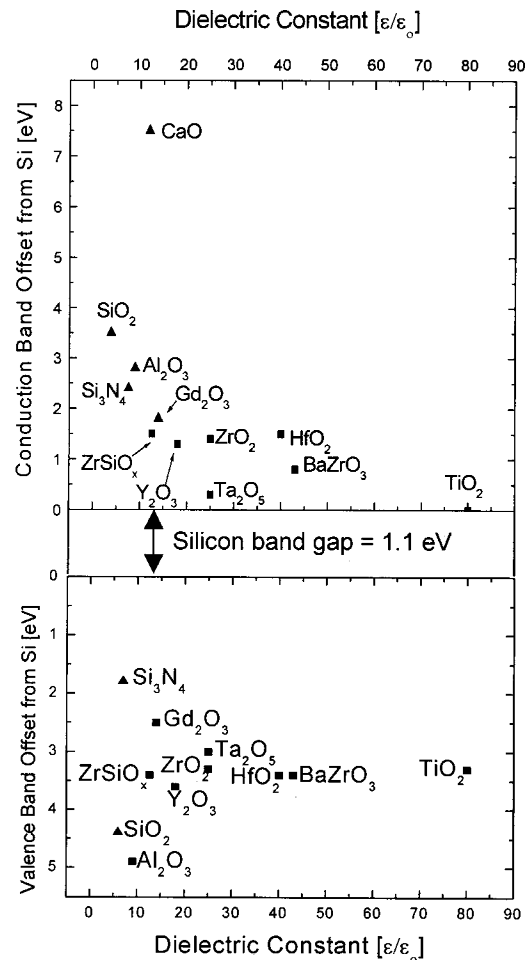

FIG. 2. Shows the relationship between the dielectric constant and band offset from Si for various materials. The upper panel shows the conduction band offsets and the lower panel shows the valence band offsets. They are separated by a silicon band gap of 1.1 eV. Squares indicate theoretical band offset values and triangles indicate experimental band offset values. The dielectric constants given are from recent journal articles and vary slightly according to deposition method or other factors. The values used in this figure are indicated by an asterisk in Table I.

(first and third layers) material should have a low dielectric constant. However, it is challenging to find dielectric materials that meet these requirements, because most dielectrics with high dielectric constants have low band offsets and vice versa.[11]

There are several factors that need to be taken into account when determining the appropriate materials and structures to demonstrate the proposed barrier lowering. We have focused on specific candidate structures by considering the barrier heights, dielectric constants, and thicknesses of amorphous dielectric media for which there is some fabrication experience for silicon based devices. The total barrier thicknesses that are considered are between 10 and 20 nm. Ideal barrier heights for the center layer are in the range 2.5–3.5 eV, while the outside layers should be 1.0–1.5 eV. It should be noted that the barrier height has a larger influence on the tunneling characteristics than does the dielectric constant.

Table I is a list of reported dielectric constants, band gaps, and experimental and theoretical values for the conduction and valence band offsets of various dielectric materials on Si. These offsets are shown as a function of dielectric constant in Fig. 2. This figure enables us to determine promising materials to maximize the overall barrier height lowering in layered dielectric tunnel barrier structures. For electron tunneling devices, the approximately inverse relation between conduction band offset and dielectric constant complicates the search for a material with low dielectric constant and low band offset and for another with high dielectric constant and high band offset. For hole tunneling devices, no clear trend emerges as indicated by the distribution of dielectric constants and band offsets for hole tunneling shown in Fig. 2. This could be an advantage when choosing materials for such devices.

III. RESULTS

In Fig. 3(a), tunneling electron density per unit energy is shown as a function of $E_x - E_f$ (difference between the normal component of electron energy and the Fermi level) for a 4 nm and 6 nm (3 eV height for both) barrier with a bias of 0.1 V. The curve for the 4 nm barrier (solid line) has a maximum that is about 1 eV above the Fermi level. The electron transport does not occur directly from the Fermi level, because it is being limited by the Schottky barrier caused by the silicon depletion region. For the 15 nm barrier (dotted line), it is observed that the electron transport occurs at higher energies, an indication of thermionic emission.

Figure 3(b) shows the analogous structures at a higher bias voltage of 2.0 V. For a 4 nm barrier (solid line), tunnel-

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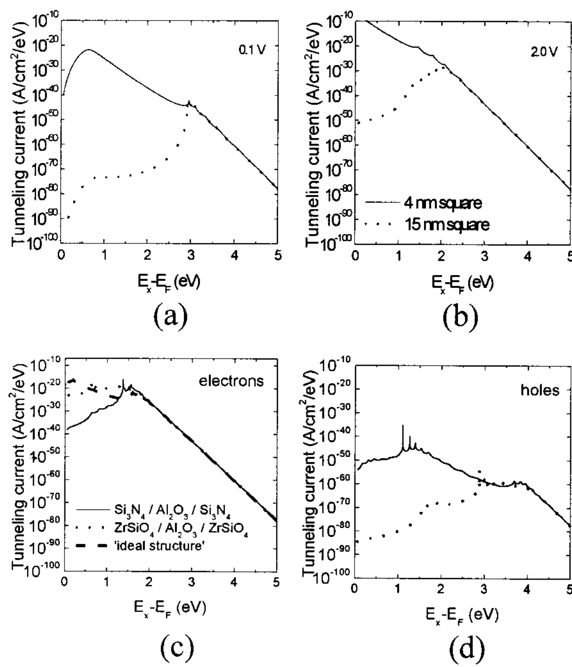

FIG. 3. Tunneling current per unit energy (A/cm^2/eV) as a function of $E_x - E_F$ (eV). The solid line in part (a) is for a 3 eV, 4-nm-square barrier and the dotted line indicates a 3 eV, 15-nm-square barrier at a bias of 0.1 V. Part (b) shows the analogous situation for a bias of 2.0 V, while part (c) shows the transport of electrons through three different three-layer tunnel barriers. The solid curve indicates $Si_3N_4/Al_2O_3/Si_3N_4$. The dotted curve indicates $ZrSiO_x/Al_2O_3/ZrSiO_x$. The dashed curve indicates an ideal structure with barrier heights 1.0/3.0/1.0 eV and dielectric constants 7.5/9.0/7.5. The thickness of each individual dielectric layer is 6 nm. Part (d) shows the analogous cases for the tunneling of holes. A bias of 2.0 V is applied in each case.

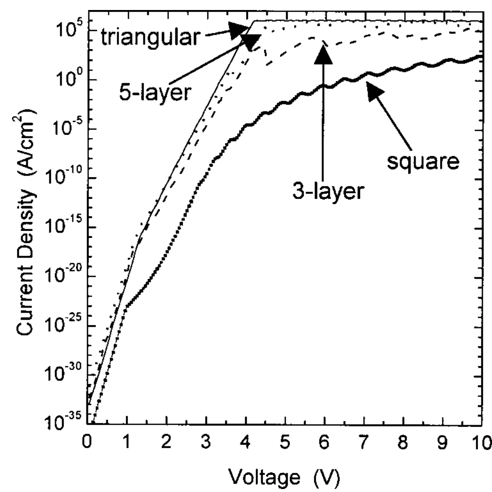

FIG. 4. Simulated $I-V$ curves for various tunnel barriers. The solid line shows an $I-V$ curve for a continuously graded triangular barrier (2.5 eV band offset and 20 nm thick). The dotted line represents a theoretical five-layer structure with band offsets of 1.0/1.6/2.5/1.6/1.0 eV and 4 nm individual thicknesses. The dashed line is a theoretical three-layer structure with band offsets 1.4/2.5/1.4 eV and thicknesses 7/5/7 nm. The line with squares represents an 8 mm square barrier with a 2.5 eV band offset.

ing is still the dominant transport mechanism. The maximum tunneling current is at $E_x - E_f = 0$, meaning that most of the transport occurs at the Fermi level. For the 15 nm barrier, the increase in voltage causes the maximum tunneling current to be shifted to lower energies as is shown by the dotted line in Fig. 3(b). The transport in this case is still dominated by thermionic emission; the shift to lower energy transport (compared with the 0.1 V case) is due to the lowering of the barrier maximum.

We have calculated the tunneling current density per unit energy versus $E_x - E_f$ for three candidate three-layer structures: $Si_3N_4/Al_2O_3/Si_3N_4$, $ZrSiO_x/Al_2O_3/ZrSiO_x$, and an "ideal" structure (meaning it shows a large current ratio) with barrier heights 1.0/3.0/1.0 eV and dielectric constants of 7.5/9.0/7.5. The results of these calculations are shown in Fig. 3(c). The assumed barrier conduction band offsets with respect to silicon are 2.4 eV for Si_3N_4 and 2.8 eV for Al_2O_3, and the dielectric constants for Si_3N_4 and Al_2O_3 are 7.5 and 9.0, respectively. $ZrSiO_x$ has a conduction band offset of 1.5 eV and a dielectric constant of 12.6.[7] The thickness for each dielectric layer in the structure is 6 nm and the applied voltage is 2.0 V. The dashed curve in Fig. 3(c) describes the ideal structure, and shows such significant barrier lowering that the electrons can tunnel through the structure directly from the Fermi level. For comparison, the heterostructure that incorporates Si_3N_4 [the solid curve in Fig. 3(c)] shows a maximum in tunneling current at about 2 eV under the same applied voltage of 2.0 V. This behavior results from the relatively small difference in barrier heights for the two materials (only 0.4 eV) and indicates that the barrier to electron transport at this applied voltage is effectively thicker than the ideal structure, allowing electron transport only at higher energies to occur over the structure (thermionic emission). The $ZrSiO_x$ structure [dotted curve in Fig. 3(c)] shows an intermediate behavior with a smaller tunneling electron current directly from the Fermi level than for the ideal structure, but greater than for the Si_3N_4 structure.

Figure 3(d) illustrates the hole tunneling behavior in $Si_3N_4/Al_2O_3/Si_3N_4$ and $ZrSiO_x/Al_2O_3/ZrSiO_x$ heterostructures. The valence band offset for Si_3N_4 is 1.8 eV while the offset for Al_2O_3 is 4.9 eV. $ZrSiO_x$ has a valence band offset of 3.4 eV. In the $Si_3N_4/Al_2O_3/Si_3N_4$ structure, the maximum hole transport occurs at energies that are just above the Fermi level of the silicon. This is due to the large differences in the valence band offsets for the Si_3N_4 and Al_2O_3. The maximum tunneling current occurs at higher energies for the $ZrSiO_x/Al_2O_3/ZrSiO_x$ structure, although two steps in tunneling current can be observed (dotted curve). The first step in tunneling current indicates the change in electron transport from tunneling to thermionic emission over the first barrier, while tunneling remains dominant through the second barrier. The second step indicates that the electron transport is not limited by tunneling in any part of the structure and the electrons are being thermionically emitted over the entire barrier. To a lesser degree these steps can be observed in the $Si_3N_4/Al_2O_3/Si_3N_4$ structure. Resonances can be observed and result from the potential wells formed between the layers when the bias is applied.

As described in Eq. (2), by integrating over all energies, the total current can be obtained. In Fig. 4, several simulated $I-V$ curves for theoretical barrier structures are shown that closely approximate a perfectly graded barrier. A graded, triangular barrier structure (2.5 eV maximum band offset, 20 nm thick) is shown by the solid curve. A five-layer structure

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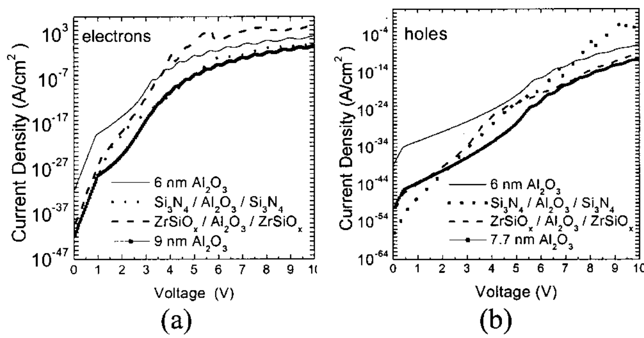

FIG. 5. Simulated $I-V$ curves for structures of Al_2O_3, Si_3N_4, and $ZrSiO_x$ Part (a) shows $I-V$ curves for electrons, where the solid curve shows tunneling through 6 nm Al_2O_3, the dotted curve is for $Si_3N_4/Al_2O_3/Si_3N_4$ (6 nm each), the dashed curve is for $ZrSiO_x/Al_2O_3/ZrSiO_x$ (6 nm each), and the curve with squares is for 9 nm Al_2O_3. Part (b) shows $I-V$ curves for holes, where the solid curve is for 6 nm Al_2O_3, the dotted curve is for $Si_3N_4/Al_2O_3/Si_3N_4$ (6 nm each), the dashed curve is for $ZrSiO_x/Al_2O_3/ZrSiO_x$ (3 nm each), and the curve with squares is for 7.7 nm Al_2O_3.

($\Delta\varepsilon_c$: 1.0/1.6/2.5/1.6/1.0 eV, 4 nm individual layer thickness) is shown by the dotted line and its tunneling characteristics very closely approximate the continuously graded barrier. The dashed line shows a three-layer structure ($\Delta\varepsilon_c$: 1.4/2.5/1.4 eV, $t=7/5/7$ nm) whose behavior still approximates the graded structure, but differs more than the five-layer structure. A square barrier ($\Delta\varepsilon_c$: 2.5 eV, $t=8$ nm) is represented by the line with square symbols. Its tunneling characteristics are considerably different from the graded and layered barriers exhibiting an electron tunneling current density at $V=4$ V, approximately 10^{11} times lower. Curves such as these emphasize the ability of layered structures to significantly increase the tunneling current ratios compared with the square barriers that are used in devices today. Though it may be very difficult to find materials to construct the five-layer barriers, it is interesting to see how closely they approximate the graded barrier.

The simulated ($I-V$) curves for $Si_3N_4/Al_2O_3/Si_3N_4$ and $ZrSiO_x/Al_2O_3/ZrSiO_x$ on n-type silicon are shown in Fig. 5(a). Under a 4.0 V bias, for the Si_3N_4 three-layer structure with 6 nm of each material, we expect a current ratio of 10^{31}, while we expect a current ratio of 10^{25} for a single 6 nm homogeneous barrier of Al_2O_3, although most of the current is limited by the Schottky barrier in this case. The current ratio for the $ZrSiO_x$ layered structure, is larger (10^{37}) due to the greater difference in barrier heights. For comparison, a 9 nm Al_2O_3 layer gives a current ratio of 10^{31}, although the total electron tunneling current is lower for this case.

The differences between homogeneous barriers and layered barriers on p-type silicon are shown in Fig. 5(b). We again examine the results from a 4.0 V bias: for the 6 nm Al_2O_3 barrier, we see a current ratio of 10^{14}, whereas a 7.7 nm Al_2O_3 barrier gives a current ratio of 10^{16}. The $ZrSiO_x$ layered barrier gives a greater current ratio of 10^{23}. The simulated current ratio is quite dramatic for the Si_3N_4 layered barrier (10^{28}) because of the significant difference in the band offsets compared to that of silicon for the two materials.

Other fabrication issues to be considered include defect density and interface quality. Localized trap states within the barrier films might result in bias dependent leakage currents that could obscure the barrier lowering effect. Likewise, if an unwanted (e.g., silicon dioxide) film develops at the silicon–barrier interface, a spurious barrier with large barrier height and relatively low dielectric constant could cause the speed of the program/erase process to decrease. In our analysis, we have focused on amorphous materials. Such materials are of particular interest because they are simple to fabricate on silicon compared with the growth of lattice constant matched crystalline materials.

IV. CONCLUSION

In summary, we have explored the performance of silicon based layered tunnel dielectric barrier structures and have predicted the tunneling characteristics for various barrier physical parameters. Our model indicates the dominant current transport mechanism for different barrier structures and shows that five- and three-layer barriers closely approximate the perfectly graded barriers, giving promise for these structures to be integrated into silicon based technology. We have comprehensively surveyed the dielectric constants and band offsets for dielectric materials that are under investigation in recent literature. Based on this data and on our simulations, two real structures that could potentially demonstrate the barrier lowering effect are $Si_3N_4/Al_2O_3/Si_3N_4$ and $ZrSiO_x/Al_2O_3/ZrSiO_x$. Compared with similar devices that utilize homogeneous tunneling barriers, layered barriers could improve both the speed and retention time of floating gate memory devices.

ACKNOWLEDGMENTS

This work was supported by the National Science Foundation and the NASA CETDP program.

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