EFFECT OF DEFECT-RICH EPITAXY ON CRYSTALLINE SILICON / AMORPHOUS SILICON HETEROJUNCTION SOLAR CELLS AND THE USE OF LOW-MOBILITY LAYERS TO IMPROVE PEFORMANCE

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ABSTRACT

We present two-dimensional device physics simulations of amorphous silicon / crystalline silicon heterojunction solar cells to explain the effects of full and localized epitaxial layers, sometimes observed in the early stages of amorphous Si deposition, on cell performance. Minimizing the defect density, thickness, and wafer area fraction covered by the epitaxial region are shown to be important factors for maximizing cell open circuit voltage. We find that localized defect-rich epitaxial patches covering small percentages of the wafer surface (~5%) can cause significant reduction in open circuit voltage, which is explained by considering lateral carrier flow in the device. We also show that a thin layer of low-mobility material, such as microcrystalline silicon, included between the wafer and amorphous regions can impede lateral carrier flow and improve conversion efficiencies in cases where isolated defective pinholes limit device performance.

INTRODUCTION

Crystalline silicon (c-Si)/ amorphous silicon (a-Si) heterojunction cells, also known as HIT-cells (heterojunction with intrinsic thin layer), offer a promising route toward low-cost, high-efficiency Si photovoltaics. They can be fabricated from Si wafers at low temperature, and the heterojunction allows for a high open circuit voltage (V_{oc}). Such cells are typically fabricated from c-Si wafers, and have a-Si emitter, back surface field, and intrinsic layers deposited by plasma enhanced chemical vapor deposition (PECVD) or sometimes hot-wire chemical vapor deposition (HWCVD).

It is well known from experiments that to optimize photovoltaic conversion efficiency, care must be taken to control the a-Si/c-Si interfaces in HIT-cells. Numerical modeling and experiments have shown that recombination and charging due to interface defects can degrade performance [1-4]. Along with the passivation of these interface defects, it has been shown experimentally that avoiding epitaxy during the early stages of a-Si deposition is also critical to high performance [5-8]. It has been proposed that this is due to poor quality of the epitaxy leading to recombination.

Here we implement two-dimensional device simulations to study the effects of these epitaxial layers. We model devices with a defect-rich epitaxial layer covering the full wafer surface, and also those with isolated regions of epitaxy. We show that even when defect-rich epitaxy is confined to a small percentage (~5%) of the wafer surface, performance can be significantly degraded and we describe the device physics governing this effect. Finally, we consider the inclusion of a thin layer of low-mobility microcrystalline Si (μc-Si) to reduce lateral carrier flow toward defective pinhole regions and improve device performance.

SIMULATION DETAILS

The simulated cell is based on a 200 μm thick n-type Si wafer doped at 10^{16} cm^{-3}. The layer structure from front to back is a-Si(p)/a-Si(i)/c-Si(n)/a-Si(i)/a-Si(n) with Ohmic front and back contacts. The doped a-Si regions are doped at 3×10^{19} cm^{-3}. For the basic cell, in which no epitaxy is present, all a-Si layers are 5nm thick. To model the effect of partial epitaxy, an additional c-Si layer is included so the front junction layer structure is a-Si(p)/a-Si(i)/c-Si(epi)/c-Si(n), or a-Si(p)/c-Si(epi)/c-Si(n) for the cases where epitaxy extends into the emitter region. The combined thickness of the amorphous and epitaxial layers is fixed at 10 nm. The first 5 nm of crystalline epitaxy is assumed to be intrinsic, and the additional epitaxy is doped at the same level as the a-Si emitter. We also consider isolated regions of epitaxy in which the epitaxial region only covers a portion of the front junction, the rest retains the a-Si(p)/a-Si(i)/c-Si(n) structure. The simulated structure is illustrated in Figure 1. For all results presented here the simulation region width, and thus the effective pitch between isolated epitaxial regions, is 500 nm.

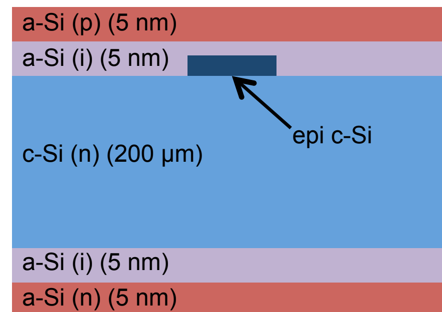

Figure 1: The HIT-cell structure used for device simulations. Defects are included in the epitaxial c-Si region for which the width and thickness are varied.

The electrical behavior of the heterojunctions is simulated taking into account thermionic emission and tunneling at interfaces according to the Wentzel–Kramers–Brillouin (WKB) approximation as implemented in the software package Sentaurus Device based on the approach in Ref [9]. Tunneling has been shown to be an important consideration for a-Si/c-Si heterojunctions [2]. The electrical properties and band structure parameters for a-Si are taken from Ref [10], with recombination in the a-Si regions modeled based on the explicit inclusion of band tail and Gaussian dangling bond traps according to the parameters presented in Ref [10]. Shockley-Read-Hall (SRH) recombination is assumed in the Si wafer region with electron and hole lifetimes of 100 µs. To model the effect of defects incorporated into the c-Si epitaxial layers, we include varying densities of mid-gap traps (both acceptor and donor) with capture cross sections of 10^{-15} cm^{-2} in the epitaxial region. The full electrostatics and recombination statistics of the traps in both the epitaxial and a-Si layers are included. Doping dependent mobility and Auger recombination are also taken into account in the crystalline Si regions. Fermi statistics is implemented for the entire structure.

In order to study the effects of including a layer with reduced mobility near the front junction, a region of µc-Si varying in thickness from 10 nm to 100 nm is included just below the front a-Si / defective c-Si layer. The combined thickness of the wafer and µc-Si is fixed at 200 µm. The electron and hole mobilities in this region are estimated to be 5 cm^2 V^{-1} s^{-1} and 1.65 cm^2 V^{-1} s^{-1}, respectively. Recombination is included in this layer with electron and hole SRH recombination lifetimes varied from 1 ns to 100 ns. All other properties of this layer including the doping level are assumed to be the same as in the c-Si wafer.

We carry out the two-dimensional numerical simulations of these structures with Synopsis TCAD including Sentaurus Device physics simulator. The carrier generation profile is calculated based on a single pass of AM1.5G illumination binned in 95 discrete wavelengths. The optical properties of a-Si are taken from spectroscopic ellipsometry measurements of a-Si films. Current-voltage curves are generated by varying voltage across the contacts and numerically solving the Poisson and carrier transport equations on a finite-element mesh for each voltage.

RESULTS

Effects of defective epitaxial regions

We first consider the case in which the defect-rich epitaxial layer covers the entire wafer surface. We perform simulations for different epitaxial layer thicknesses and defect densities. Figure 2 shows V_{oc} as a function of epitaxial layer thickness for several values of the defect density. We find that V_{oc} is not significantly degraded until the defect density in the epitaxial layer exceeds 10^{17} cm^{-3}. We also note that as the thickness of the defective epitaxial layer increases, performance is degraded in agreement with experimental reports in the literature [5-7]. Once the defect density reaches ~10^{19} cm^{-3}, the V_{oc} becomes severely degraded and is suppressed below 500 mV once the epitaxy extends into the doped layer.

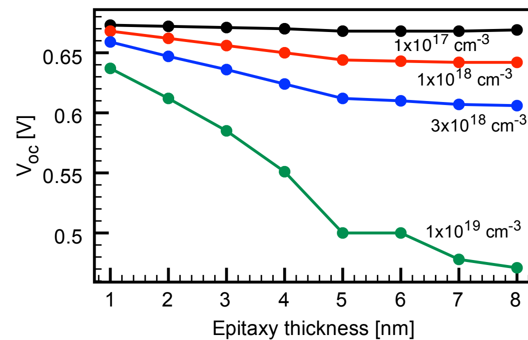

Figure 2: Simulated open circuit voltage as a function of epitaxial thickness for defect-rich epitaxial layers covering the entire wafer at the front heterojunction for varying values of mid-gap trap density (as labeled) in the epitaxial layer.

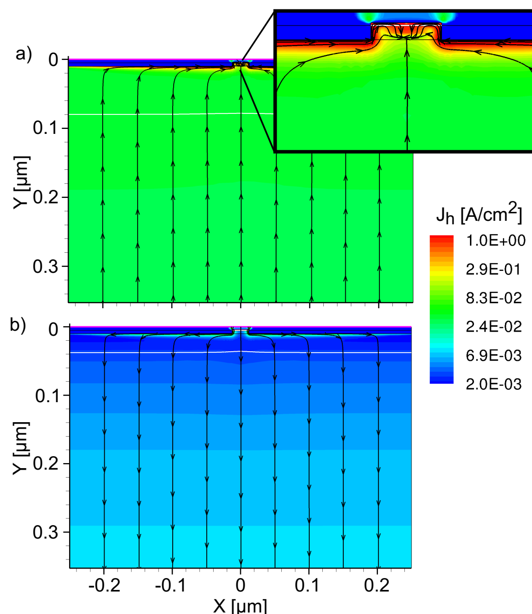

Figure 3: Modeling results showing the magnitude and direction of the hole current density (J_h) under illumination at open circuit at the front of the device for a 25 nm wide 6 nm thick epitaxial region for two cases: (a) mid-gap trap density in the epitaxial region of 1 x 10^{19} cm^{-3} with the inset showing a magnified view of the localized epitaxy and (b) defect-free epitaxial region. The horizontal white lines indicate the edge of the depletion region. The black lines and arrows indicate only the direction of current flow.

We next explore the effects of localized epitaxy on the wafer surface. Figure 3 shows the hole (the minority carrier type in the wafer) current density at open circuit for a structure in which a 6 nm thick epitaxial region covers 25

nm of the wafer surface. This corresponds to 5% coverage since the simulated region is 500 nm wide. Figure 3a shows the case in which the epitaxial region has a defect density of 10^{19} cm^{-3}, and the device achieves a V_{oc} of 588 mV, while Figure 3b shows the hole current density for the same geometry but with a defect-free epitaxial layer at its V_{oc} of 674 mV. We see that the open circuit condition is met in the defective case (Figure 3a) with holes flowing toward the front of the cell where they turn and flow along the a-Si/c-Si interface toward the defective epitaxial region. This is in contrast defect-free case, which exhibits a significantly lower hole current density in the wafer flowing toward the rear of the device; the direction holes would flow in a forward biased diode in the dark.

We can understand this behavior by noting that the epitaxial region provides a lower-resistance pathway for carrier collection than the thick a-Si regions, so carriers tend to flow through the epitaxial region. If this region is defect-rich, those carriers are subject to recombination before reaching the contact. Thus, the open circuit condition is reached at a lower voltage, even though there remains a significant flow of photogenerated carriers in the wafer toward the front junction.

Figure 4 summarizes how the presence of localized defect-rich epitaxy affects cell performance across a range of parameters. Figure 4a illustrates that the primary effect on increasing defect density in the epitaxial region is to limit the V_{oc}. In agreement with the microscopic explanation presented above, Figure 4b shows that V_{oc} can be significantly degraded in the presence of highly defective epitaxy, even if the epitaxial region is confined to a small percentage of the wafer surface. The results presented in Figure 4b also indicate that this effect is intensified for thicker epitaxial layers. We suggest that this is due to increased carrier flow through the epitaxial region because of even lower resistance in these thicker epitaxial regions than in thinner ones.

Reduced-mobility layers to improve efficiency

It has previously been shown using equivalent circuit modeling that increased distributed series resistance can limit the detrimental effects of spatial nonuniformities in the electrical properties of solar cells [11]. Here, the observation of lateral carrier flow in the wafer toward the defective epitaxial regions suggests that limiting the carrier mobility in the region just below the heterojunction may act to mitigate the effects of the defective epitaxial regions in a similar manner. We investigate this possibility by including a region of reduced mobility, in this case μc-Si, between the wafer and the a-Si regions as illustrated in Figure 5a. Here, we refer to the defective crystalline regions protruding into the a-Si layers as pinholes, since they can no longer be understood as epitaxial with respect to the wafer. Similar approaches have incorporated resistive nanocrystalline silicon oxide layers near contacts in thin-film Si cells to mitigate shunt pathways in aggressively textured geometries [12, 13].

We find that in cases of moderate to high defect level within the pinhole region, the inclusion of 20 nm to 40 nm of low-mobility μc-Si below the heterojunction can improve overall energy conversion efficiency, even when the carrier lifetime in the μc-Si layer is limited to 1 ns (Figure 5b). These improvements are substantial and exceed 4% absolute efficiency in the case of highly defective pinhole regions (N_t = 3x10^{19} cm^{-3} in Figure 5b). Care must be taken in applying this approach because the introduction of a μc-Si layer can degrade performance in cases where the defective pinhole is not strongly degrading performance (N_t = 3x10^{18} cm^{-3} in Figure 5b). In addition, efficiency is degraded if the reduced-mobility layer is made too thick, especially when carrier lifetime in that layer is low. It is important to note that there will be experimental challenges related to the deposition of the a-Si films on a μc-Si layer. In general, the microstructure of the a-Si layer is coupled to the underlying substrate or μc-Si film. However, the inclusion of such mobility limiting layers remains a promising strategy to reduce the effects of defective pinhole-like structures in heterojunction solar cells.

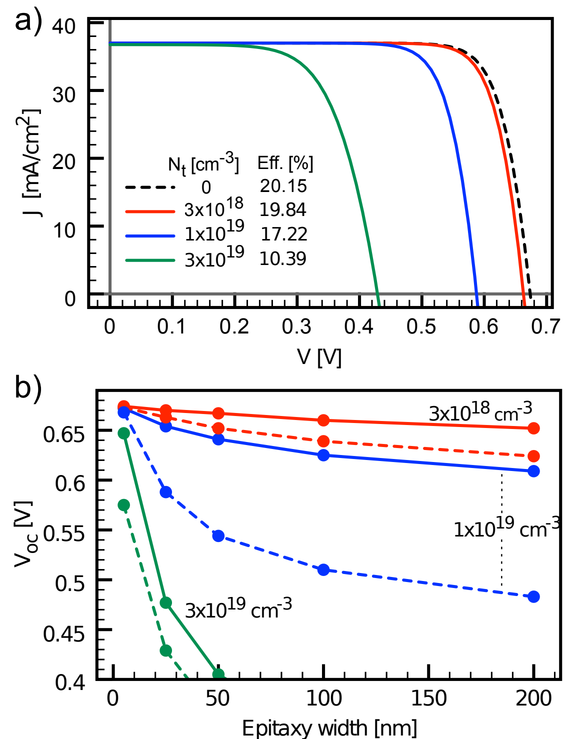

Figure 4: a) Simulated current-voltage curves and conversion efficiencies for cells with a 6 nm thick, 25 nm wide epitaxial region for changing values of mid-gap trap density (N_t) in the epitaxial region. b) Simulated open circuit voltages under illumination as a function of epitaxy width for 3 nm (solid lines) and 6 nm (dashed lines) thick epitaxial regions for varying values of N_t as labeled and indicated by color.

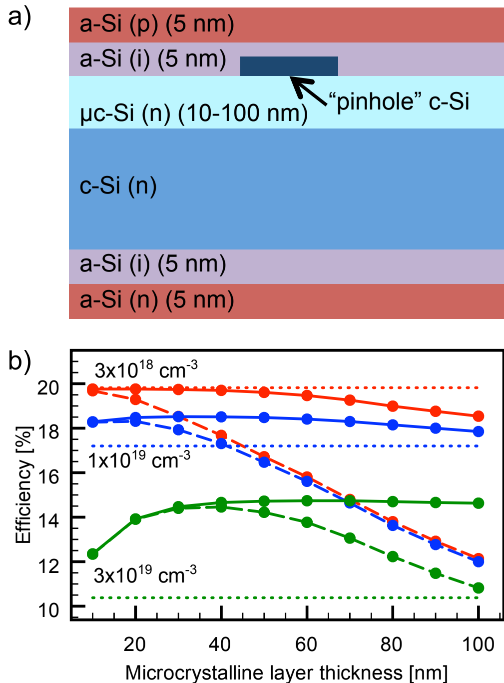

Figure 5: a) The layer structure modeled when considering the use of reduced-mobility layers. The pinhole region has the same properties as the epitaxial region considered above. b) Simulated solar conversion efficiencies for varying thickness of the μc-Si reduced-mobility layer for three values of N_t, indicated by color as labeled. Solid and dashed lines indicate SRH lifetimes in the μc-Si of 100 ns and 1 ns respectively. The horizontal dotted lines represent the efficiencies of devices with identical pinholes of given N_t but without a μc-Si layer. The pinhole region is 6 nm thick and 25 nm wide.

CONCLUSION

The numerical model presented here improves our understanding of how defect-rich epitaxy on the wafer surface during a-Si layer deposition, even in localized areas, can degrade the performance of c-Si/a-Si heterojunction solar cells. Our results highlight the importance of detailed microstructural characterization in these devices, and illustrate important effects that can only be captured in two- and three-dimensional modeling. It also demonstrates that including regions of degraded mobility near the heterojunction enhance cell performance by limiting lateral carrier flow toward defective pinholes in the heterojunction. This design strategy may be made even more powerful with careful control of anisotropy in the carrier mobility of the reduced-mobility region by, for example, taking advantage of columnar-grained microstructures. Further understanding of heterojunction performance through modeling and the inclusion of mobility-limiting layers will aid in advancing the c-Si/a-Si heterojunction solar cell platform and will further benefit from continuing advances in the characterization of the heterojunction interface.

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