Design and Growth of III-V on Si Microwire Array Tandem Solar Cells

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***Abstract* — Tandem $Ga_{1-x}In_xP$/Si microwire array solar cells are a route towards a high efficiency, low cost, flexible, wafer-free solar technology. Coupled full-field optical and device physics simulations of a $Ga_{0.51}In_{0.49}P$/Si wire array tandem are used to predict device performance. A 500 nm thick, highly doped "buffer" layer between the bottom cell and tunnel junction is assumed to harbor a high density of lattice mismatch and heteroepitaxial defects. Under simulated AM1.5G illumination, the device structure explored in this work has a simulated efficiency of 23.84% with realistic top cell SRH lifetimes and surface recombination velocities. The relative insensitivity to surface recombination is likely due to optical generation further away from the free surfaces and interfaces of the device structure. To move towards realizing these device structures, GaP and $Ga_{1-x}In_xP$ layers were grown heteroepitaxially with metalorganic chemical vapor deposition on Si microwire array substrates. The layer morphology and crystalline quality have been studied with scanning electron microscopy and transmission electron microscopy, and they provide a baseline for the growth and characterization of a full device stack.**

***Index Terms* — epitaxial layers, III-V semiconductor materials, semiconductor device modeling, silicon**

I. Introduction

Si microwire arrays [1] are a promising route to realizing a flexible, wafer-free single junction photovoltaic technology. After growth and junction formation on a patterned Si wafer, wire arrays can be infilled with Polydimethylsiloxane (PDMS) and released from the substrate with a razor blade [2]. The arrays, despite their small projected area, are capable of absorbing as much as a planar Si slab with 100 times the volume [3]. Small area wire array devices have shown promise in both photovoltaic and photoelectrochemical applications [4]-[5].

Based upon the performance of existing devices, the upper bound on energy conversion efficiency in single junction Si wire arrays is only 17% [6]. Integration of III-V top cells directly on wire array cells can greatly increase the efficiency potential, while retaining many of the benefits of the wire arrays. Prior computational modeling work has resulted in a lattice matched GaAsP/SiGe wire array tandem device design with 27% efficiency [10].

Heteroepitaxially grown GaP on Si, being nearly lattice-matched, remains an area of research interest for the integration of III-V materials as active optoelectronic devices on Si. Pristine, anti-phase domain free material has only been grown with carefully optimized nucleation on pristine Si(001) substrates [7]-[8]. The geometry of the Si microwires, grown in the (111) direction with (112) and (110) sidewalls, present a significant challenge to the growth of GaP and other III-V alloys [9]. Recent efforts in mismatched heteroepitaxy of Ge on Si nanopillars suggest that in the wire geometry defects in heteroepitaxial layers can be grown out close to the interface between the two materials [11].

In this work, we present simulation results of a lattice mismatched $Ga_{0.51}In_{0.49}P$/Si wire array tandem device design and initial results in the metalorganic chemical vapor deposition (MOCVD) growth of GaP and $Ga_{1-x}In_xP$ step graded layers on wire arrays.

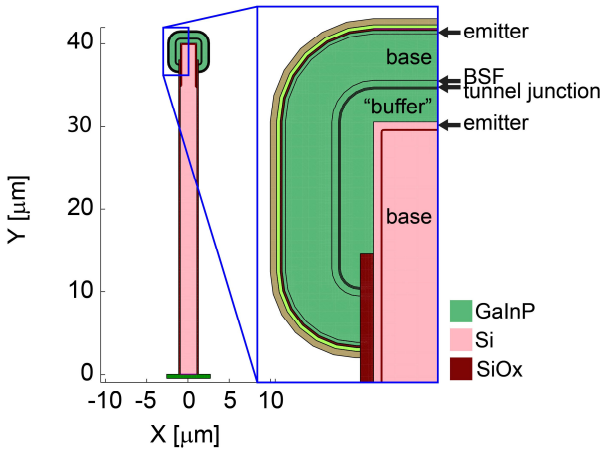

Fig. 1. Detail of the simulated 2D device geometry. A 500 nm thick highly doped $Ga_{0.51}In_{0.49}P$ "buffer," considered to be where defects are grown out of the III-V material and therefore highly defective, bridges the heteroepitaxial interface between the Si wire bottom cell and the III-V top cell structure.

II. Tandem Device Design

For a Si bottom cell, an ideal top cell with a bandgap of 1.7 eV, such as ordered $Ga_{0.45}In_{0.55}P$ or disordered $Ga_{0.35}In_{0.65}P$ alloys, would yield a detailed balance efficiency of 41%. Our simulated device incorporates a $Ga_{0.51}In_{0.49}P$ top cell with a bandgap of 1.89 eV, which results in a detailed balance efficiency of 35%. $Ga_{0.51}In_{0.49}P$ cells with $Al_{0.5}In_{0.5}P$ window layers, utilized successfully in high efficiency triple junction solar cells for several years, have been studied thoroughly and thus lend themselves to realistic predictions of device performance despite lower efficiency potential.

TABLE I

DEVICE PARAMETERS OF SIMULATED WIRE ARRAY TANDEM

Layer	Properties
ARC	55 nm TiOx, 95 nm MgF
Window	$Al_{0.5}In_{0.5}P$, n = $2x10^{18}$ cm^{-3}, 30 nm
Emitter	$Ga_{0.51}In_{0.49}P$, n = $2x10^{18}$ cm^{-3}, 50 nm
Base	$Ga_{0.51}In_{0.49}P$, p = $1.2x10^{17}$ cm^{-3}, 700 nm
BSF	$Ga_{0.51}In_{0.49}P$, p = $4x10^{17}$ cm^{-3}, 100 nm
Tunnel junction	$Ga_{0.51}In_{0.49}P$, p = $1x10^{19}$ cm^{-3}, n = $4x10^{-19}$ cm^{-3}, 30 nm
Buffer	$Ga_{0.51}In_{0.49}P$, n = $1.8x10^{18}$ cm^{-3}, 500 nm, τ_{SRH} = 1 ps
Si wire emitter	Doping dependent τ_{SRH}, Gaussian doping function with n = $1x10^{19}$ cm^{-3} peak value, extends 5 μm downward from wire tip
Si wire base	τ_{SRH} = 1 μs, p = $1x10^{17}$ cm^{-3}, 2 μm diameter, 40 μm tall, 5.3 μm array pitch
Back reflector	Perfect electrical conductor

The device structure (Fig. 1) was chosen to mimic experimentally observed geometries and other experimental constraints. In particular, a 200 nm thick thermal oxide (SiOx) is patterned on the sidewalls of the Si wire, leaving only the top 2 μm of the wire in contact with the top cell. This layer is used as a mask for selective epitaxy only at the very ends of the wire. Additionally, a 500 nm thick, highly defective, heavily doped "buffer" layer has been introduced between the Si wire bottom cell and the tunnel junction. The 3.9% lattice mismatch with the Si bottom cell will result in defects due to the need for strain relief in the III-V top cell. It is assumed that any defects due to lattice mismatch and heteroepitaxy are concentrated in this region, with the consequence of low material quality. A summary of the layer materials, doping levels and geometric parameters in the full device stack is given in Table 1.

Optical and device physics models were carried out using the Synopsys Sentaurus TCAD package. Sentaurus EMW, a full field, finite difference time domain (FDTD) electromagnetic simulation tool was used to simulate the optical properties of the full device structure in 2D. To mimic a wire array, horizontal boundaries were assumed to be periodic, with a back reflector modeled as a perfect electrical conductor and a perfectly matched layer above the structure. Shockley-Reed-Hall (SRH) recombination was considered in all of the layers, while Auger and radiative recombination were also considered in each of the III-V layers. Doping dependent mobility and lifetime were also considered in the GaInP and Si, while constant mobility was assumed for the AlInP. The defective buffer layer was assumed to have a low τ_{SRH} = 1 ps.

III. OPTOELECTRONIC SIMULATION RESULTS

Generation profiles for AM1.5G illumination were computed by simulating the 2D device behavior under illumination by a plane wave of different wavelengths between 400 and 1100 nm in 50 nm increments at normal incidence (Fig. 2). Appropriate weighting parameters from a binned AM1.5G spectrum were applied to each of the simulated wavelengths to create optical generation profiles (3). In the considered geometry, the top and bottom cells absorb light equivalent to 14.2 mA/cm^2 and 16.2 mA/cm^2 respectively, compared to the 16.9 mA/cm2 and 25.3 mA/cm2 available from the above bandgap spectral bins for each cell in the AM1.5G spectrum. Losses from the window (1.02 mA/cm^2) and buffer layers (1.6 mA/cm^2) limit the top cell current. Increasing the top cell thickness should recoup the light absorption lost to the buffer layer. Bottom cell light absorption could enhanced by increasing the wire length and incorporating Al_2O_3 scatterer particles as described in [3]. These improvements are being explored in our ongoing work.

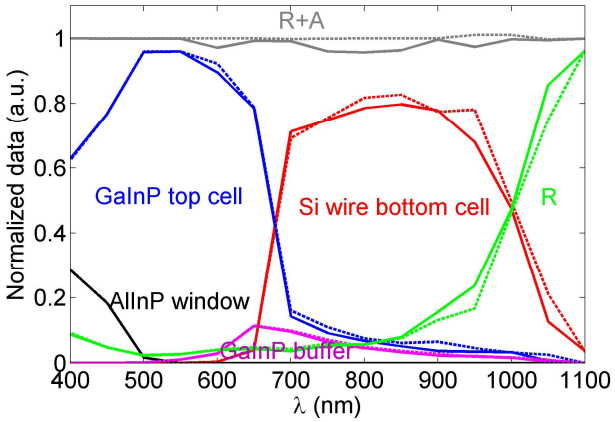

Fig. 2. Fraction of light reflected and absorbed in different parts of the device stack under TE and TM (solid and dashed, respectively) polarized plane wave illumination.

First, the effect of SRH lifetime in the top cell on performance was considered. The surface recombination velocities (SRV's) of all interfaces were set to 100 cm/s to limit their effect on device performance. With these conditions, the tandem structure considered is capable of exceeding 20% efficiency over a wide range of lifetime values (Table 2), with an upper limit of 22.88% efficiency with good material quality, τ_{SRH} = 1 ns. Furthermore, efficiencies greater than the predicted 17% for Si wire arrays alone are possible at sub-100 ps lifetimes.

More realistic surface recombination physics was introduced to the device simulations to better predict experimental performance. These simulations assumed 1 ns top cell SRH lifetime. The Si/SiOx interface is assumed to be well understood and reasonably passive (SRV = 100 cm/s). Several interfaces within the device stack could detract from device performance. The Si/GaInP and GaInP/AlInP interfaces could

TABLE II
TANDEM CELL PERFORMANCE AS A FUNCTION OF TOP CELL SRH LIFETIME

Top cell τ_{SRH}	10 ps	100 ps	1 ns	10 ns
FF (%)	76.86	84.38	86.87	88.86
V_{OC} (V)	1.657	1.778	1.876	1.912
J_{SC} (mA/cm^2)	12.98	14.04	14.04	14.04
Efficiency (%)	16.53	21.06	22.88	23.85

be quite recombination active [12]. The surface of the AlInP window layer, the top edge of the active device, will be another surface recombination source. However, all of these interfaces are also characteristic of a traditional planar stack. The GaInP/SiOx interface, resulting from III-V growth out and over a portion of the SiOx, is purely a result of wire geometry and cannot be passivated in-situ. Other than the Si/SiOx interface, the SRV at each of the aforementioned interfaces was changed from 100 to 10^4 cm/s. The efficiency of the structure dropped from 22.88 to 22.84%. The minimal effect of these large changes in SRV can be explained in part by the band structure, whereby minority carrier barriers, at the front surfaces of both cells and also at the back surface of the top cell, help reduce recombination statistics by repelling minority carriers. However, this does not explain the insensitivity to the 850 nm long interfaces on either side of the wire between the top cell GaInP and SiOx. Instead, the difference could be due to the greater portion of the optical generation (Fig. 3) occurring away from this interface as light is guided into the wire core by the higher index top cell material.

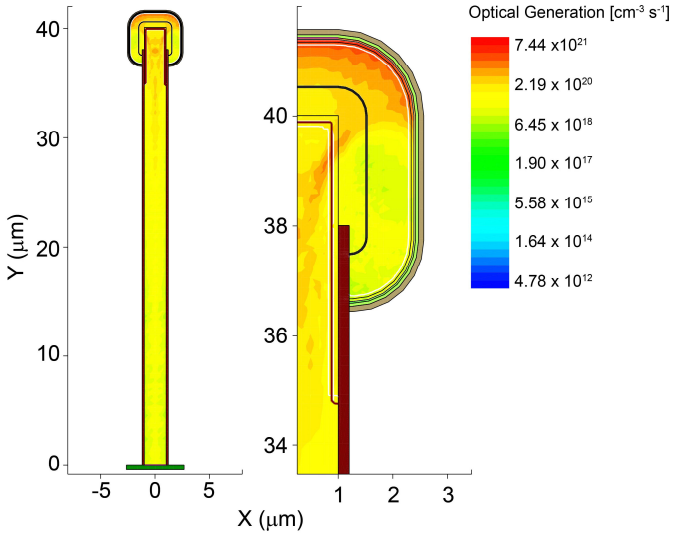

Fig. 3. Optical generation profiles generated by integration of single wavelength simulations and weighting to match the AM1.5G spectrum over the full structure (left) and inset of the top cell (right).

IV. MOCVD GROWTH OF $GA_{1-X}IN_XP$ ON SI MICROWIRES

Cu-catalyzed, vapor-liquid-solid (VLS) grown Si microwire arrays were prepared in an atmospheric pressure chlorosilane chemical vapor deposition system under H_2 ambient as described previously [1]. After growth, the masking oxide was stripped in buffered HF and the arrays were cleaned with a series of RCA1, RCA2, 30 wt. % KOH and RCA2 etches. A 100 nm thick oxide was grown on the wire array to serve as a selective epitaxy mask. The mask was defined by infilling the oxidized arrays with mounting wax, exposing the tips with an oxygen plasma ash and etching the exposed oxide with buffered HF. The remaining wax was removed in an acetone bath. Prior to MOCVD growth, wire arrays and planar controls were rinsed thoroughly in water, acetone, IPA and water before another set of RCA1 and RCA2 etches.

MOCVD growth was performed in a Thomas Swan vertical close-coupled showerhead reactor under 8 slm H_2 ambient at 100 mbar. A custom 3" quartz wafer with laser-cut 1 cm^2 windows was used to allow for growth on up to four substrates simultaneously. Substrate temperature was monitored by a pyrometer and a thermocouple in close proximity to the underside of the growth susceptor. Tertiarybutylphosphine (TBP), trimethylgallium (TMGa), and trimethylindium (TMIn) were used as group V and group III precursors. Typical growth parameters are presented in Table 3.

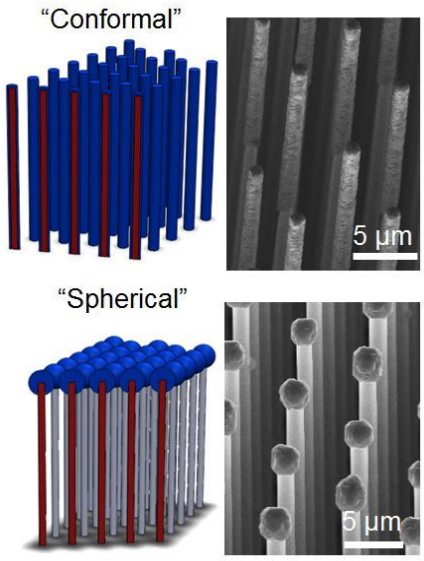

Fig. 4. The geometry of the III-V layers can be controlled by introducing a thermal oxide mask to limit the growth area, allowing full tunability between conformal and the "spherical" structures mimicked by the simulated device structure.

By tuning the height of the oxide mask, we can control the geometry of the resulting III-V layer with selective epitaxy, allowing for experimental realization of the simulated device structures (Fig. 4). Structures grown with minimal contact area between the epilayer and the Si wire cores could allow

TABLE III
TYPICAL MOCVD GROWTH PARAMETERS

	T (°C)	TBP µmol/min	TMGa µmol/min	TMIn µmol/min	V/III Ratio
GaP					
Nucleation	460	3205	61.8	-	51.9
Growth	615	3205	61.8	-	51.9
$Ga_{0.7}In_{0.3}P$					
Nucleation	460	3205	61.8	16.2	35.3
Growth	595	3205	61.8	16.2	35.3

for the rapid outgrowth or annihilation of defects close to the heteroepitaxial interface [7].

We have begun studying the growth of $Ga_{1-x}In_xP$ graded layers on Si microwires. Optimization of compositional control and growth of these layers is still underway. Initial results (Fig. 5) reveal a rich defect structure largely originating from the Si/III-V interface as well as several voids in the material. These images were used as the basis for the simulated device structures. As can be seen in the Z-contrast STEM images, each of the layers in the stack is homogeneous and continuous in extent. However, further study is necessary to understand the origin and control of these defects before realization of a full device stack.

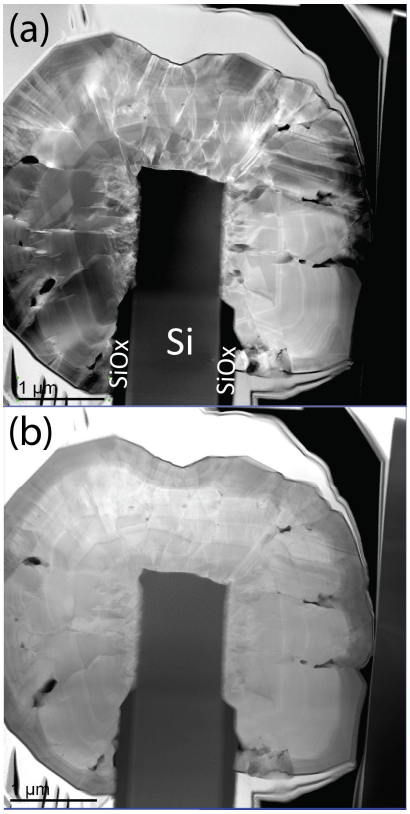

Fig. 5. $Ga_{1-x}In_xP$ and $Al_yGa_{1-x-y}In_xP$ compositionally graded layers were grown on Si microwires, with peak compositions of $Ga_{0.7}In_{0.3}P$ and $Al_{0.45}Ga_{0.35}In_{0.20}P$, and studied as axial cross sections with STEM HAADF diffraction (a) and Z contrast (b).

IV. SUMMARY

$Ga_{1-x}In_xP$ top cells grown on Si microwire array bottom cells are a candidate for a high efficiency, flexible, wafer-free tandem device. Full field optoelectronic simulations of a lattice mismatched $Ga_{0.51}In_{0.49}P$/Si wire tandem cell device structure shows promise for exceeding 20% efficiency with good top cell material quality. Despite significant possibilities for surface recombination issues at interfaces within the device stack and at the two unpassivated surfaces of AlInP and GaInP/SiOx, high SRV's of 10^4 cm/s have only a minimal effect on device performance, resulting in a drop from 22.88 to 22.84% efficiency for a top cell lifetime of 1 ns. Favorable minority carrier statistics with minority carrier blocking layers and optical generation away from these interfaces are possible explanations for the robust performance with recombination active interfaces. Meanwhile, experimental efforts in III-V selective epitaxy on Si wire arrays have been used as the motivation for implementing the simulated device geometry. Initial results in the growth of AlGaInP and GaInP graded layers on a Si wire array reveal a rich defect structure within the III-V layers. While heteroepitaxial growth of GaInP on Si microwire arrays remains a challenge, the optoelectronic device simulation and materials characterization techniques will allow for a full understanding of III-V/Si wire heterostructures.

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