# PATHS TO HIGH EFFICIENCY LOW-COST PHOTOVOLTAICS

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## ABSTRACT

We discuss approaches to approaches to synthesis of high efficiency low cost photovoltaics that employ single crystal GaAs and Si in thin film and wire array formats. A common theme is the use of lift-off processes that enable cell fabrication without consumption of a thick crystalline wafer per cell. Use of single crystal materials enables the achievement of high open circuit voltages relative to polycrystalline materials.

## INTRODUCTION

Future photovoltaic systems operating at grid parity will require simultaneously high-efficiency (>20%) and low-cost (<$0.60/Wp) photovoltaic cells and modules that also enable sharp reductions in balance-of-systems cost. Only a few photovoltaic materials and device designs currently have this potential.

Direct bandgap single-junction GaAs and III-V semiconductor thin film photovoltaics offer such a path, exemplified by the recent report of 27.6% efficiency thin film cells [1] fabricated in a very low-cost process that minimizes materials use. Even higher efficiencies are achievable by optoelectronic designs for light-trapping. Simple design coupled with a favorable temperature coefficient for photovoltaic conversion efficiency indicates that III-V semiconductor thin film photovoltaics currently have unrivaled potential for annual energy production.

Another promising photovoltaic architecture featuring high intrinsic efficiency potential, minimal material use and favorable interplay with balance-of-systems design is one based on flexible arrays of semiconductor microwires. Si microwires grown by a heterogeneously-catalyzed chemical vapor deposition process exhibit high (>90%) light absorption, high (>90%) internal quantum efficiency, and high open circuit voltages (>600mV). Cells are fabricated by templated growth of microwire arrays which are subsequently removed from a reusable single-crystal substrate via a simple peel-off process after wires have been embedded in a flexible polymer matrix. Si microwire arrays consume 1-5% of the Si of an equivalent wafer-based Si cell, but exhibit comparable optical absorption and internal quantum efficiency, owing to optoelectronic design that optimizes light trapping. Both a back reflector and mesoscale dielectric particles embedded in the polymer matrix between Si microwires enhance the optical absorption.

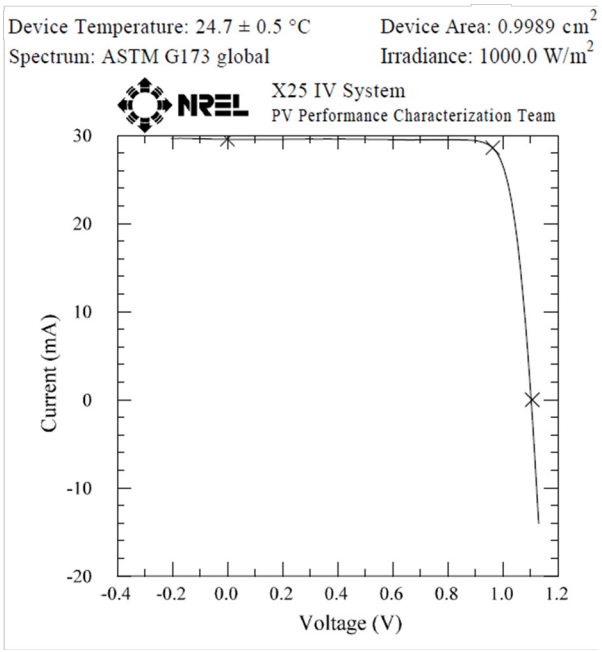


**Figure 1: Device performance characteristics of Alta Devices thin film GaAs solar cell. The 1 $cm^2$ exhibits a conversion efficiency of 27.6%, under 1 sun AM1.5G solar illumination. The cell exhibits a open circuit voltage of 1.107 V, a short circuit current density of 28.6 $mA/cm^2$ and a fill factor of 84.1%, at 25° C. (see paper by B.M. Kayes, et.al. in these Proceedings[3]).**

While current designs for III-V compound thin film cells and microwire cells have potential to meet the goal of >20% efficiency and (<0.60/Wp), future directions for even higher performance can be anticipated.

## GaAs THIN FILM CELLS

To achieve high efficiency in GaAs thin film devices, the first step is the synthesis of high quality crystalline GaAs absorber and junction layers on GaAs substrates. A thin AlAs release is grown between the GaAs substrate and cell active layers, facilitating film removal by epitaxial liftoff [2]. Following growth, the side facing away from the sun is metalized and attached to a handle substrate, and

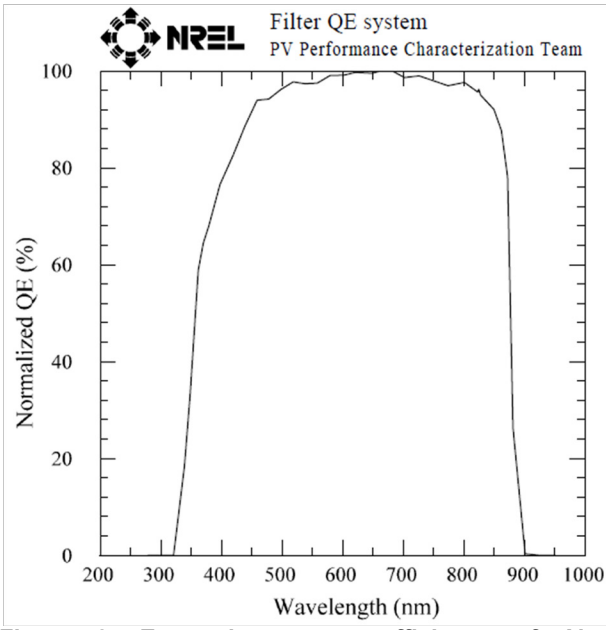


**Figure 2: External quantum efficiency of Alta Devices 1 cm$^2$ thin film GaAs solar cell at 25$^o$ C. The spectral response indicates current collection from 320-900 nm. (See paper by B.M. Kayes, et.al. in these Proceedings [3]).**

cell is removed from the substrate by epitaxial liftoff, and device processing is finished on the sun-facing side of the cell with the cell supported on the handle substrate. The device current-voltage characteristics for 1 sun illumination at 25 $^o$C are shown in Fig. 1. The open circuit voltage of 1.107 V is achievable through device design and processing that minimizes the dark current [3].

The spectral response of this GaAs thin film cell is illustrated in Fig. 2. Current collection occurs over the range 320nm – 900 nm, with mid-visible quantum efficiency close to 100%. Some loss of current collection is evident for wavelengths below 400 nm and above 800 nm, which could potentially be improved by more optimized window layer design and back reflector design, respectively. Nonetheless, this approach has yielded cell performance with an NREL-confirmed AM1.5G 1 sun conversion efficiency of 27.6% [1]; as of this writing this cell efficiency is an outright record for PV energy conversion of single-junction devices under 1 sun illumination.

Equally important for high efficiency low cost photovoltaics is power production capability under on-sun ambient conditions in which cells and modules can undergo temperatures of +/- 30$^o$ C or more away from standard test conditions at 25$^o$ C, leading to a variation of efficiency $\eta$ due to temperature variations. As a material for thin film photovoltaics, GaAs is attractive from the perspective of on-sun power generation under real-world conditions owing to its 1.42 eV direct bandgap and high material quality, leading to band-to-band generation and recombination. High quality GaAs cells can exhibit a cell temperature coefficient, $\beta = (1/\eta)\ (d\eta/dT)$, as low as 0.08%/$^o$C. Additionally, GaAs cells exhibit a lower efficiency de-rating factor at low light conditions as compared with other photovoltaic cells under low light or diffused light conditions such as high latitude deployment fields in northern Europe and Canada.

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## Si WIRE ARRAY CELLS

We have developed at Caltech a Si microwire solar cell technology that utilizes arrays of crystalline Si microwires as the active photovoltaic absorber. The wire arrays are grown using the catalytic vapor-liquid-solid (VLS) technique to seed highly controlled wire array growth in an atmospheric-pressure CVD process that produces defect-free crystalline Si wire arrays with >150 cm$^2$ area directly from gaseous $SiCl_4$. [4] We have demonstrated that high-fidelity arrays of Si microwires can be grown over large areas limited only by the size of the growth reactor, using Cu catalyst metal, in a total deposition time of < 20 min. The wires are grown on Si <111> wafers, using a patterned $SiO_2$ template layer to control the position, size, and orientation of the wires. Despite the rapid growth rate and the potential for metal contamination, the wires are defect-free, and possess minority-carrier diffusion lengths that exceed the *lengths* of the wires ($L_n$ >> 30 μm). Furthermore, studies have shown that the surfaces of the wires can be extremely well passivated ($S$ << 70 cm/s) using conventional PECVD a-Si:H or a-$SiN_x$:H films. [5]. To date, Si wire array solar cells exhibiting AM 1.5G efficiencies of $\eta$ = 8% [9] have been developed and single wire pn junction devices have

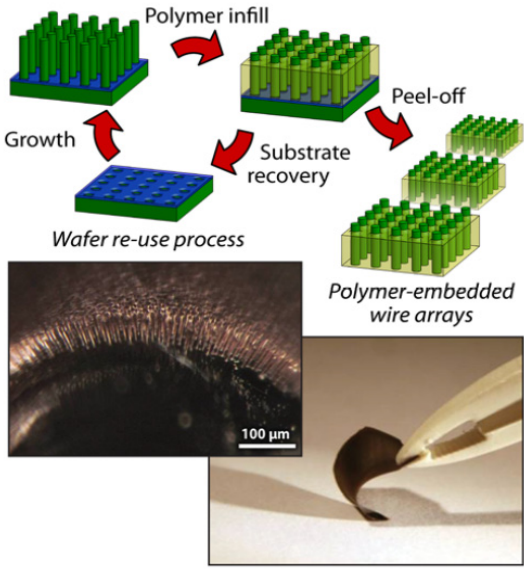


**Figure 3. Waferless Si wire array cell process utilizes array peel-off and template substrate reuse to lower cost (c.f. , ref [7]).**

exhibited $V_{OC}$ of up to 616 mV and FF of 79%[5]. Combined with optical absorption studies showing that wire arrays can absorb and collect up to 36 mA/cm$^2$ of the solar spectrum, [8] these experiments confirm that Si wire solar cells can exceed 17% efficiency even without significant further improvement in material quality or device design.

Based on experimentally measured minority-carrier diffusion lengths and surface recombination velocities, numerical device-physics simulations (including 3D electromagnetic simulations of light absorption) [4,7] predict that optimized Si wire solar cells are capable of achieving over 20% efficiency.

A mechanical peel-off procedure is used to separate the wire arrays from the growth wafer intact: The wire arrays are infilled with a liquid polymer (e.g., PDMS or EVA) and, after the polymer has cured, the composite film is simply peeled from the growth substrate using a large cutting blade. [5] This yields an optically thick, flexible sheet of high-quality c-Si of up to 120 cm$^2$ in size. To date, we have demonstrated template wafer reused up to six times [7] but expect that Si template wafer could be reused > 30 times, making their cost a very small fraction of the manufactured wire array cell cost.

## CONCLUSIONS

`Synthesis approaches for high efficiency low cost photovoltaics that employ single crystal GaAs and Si in thin film and wire array formats have potential to achieve high efficiency and low cost. . Absorber layer removal via a layer release and lift-off process permits cell fabrication to be decoupled from consumption of bulk crystalline Si and GaAs wafers.

## ACKNOWLEDGMENTS

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