Wafer-Scale Growth of Silicon Microwire Arrays for Photovoltaics and Solar Fuel Generation

Adele C. Tamboli, *Member, IEEE*, Christopher T. Chen, Emily L. Warren, Daniel B. Turner-Evans, Michael D. Kelzenberg, Nathan S. Lewis, and Harry A. Atwater

***Abstract*—Silicon microwire arrays have recently demonstrated their potential for low-cost, high-efficiency photovoltaics and photoelectrochemical fuel generation. A remaining challenge to making this technology commercially viable is scaling up of microwire-array growth. We discuss here a technique for vapor–liquid–solid growth of microwire arrays on the scale of six-inch wafers using a cold-wall radio-frequency heated chemical vapor deposition furnace, enabling fairly uniform growth over large areas with rapid cycle time and improved run-to-run reproducibility. We have also developed a technique to embed these large-area wire arrays in polymer and to peel them intact from the growth substrate, which could enable lightweight, flexible solar cells with efficiencies as high as multicrystalline Si solar cells. We characterize these large-area microwire arrays using scanning electron microscopy and confocal microscopy to assess their structure and fidelity, and we test their energy-conversion properties using a methyl viologen ($MV^{2+/+}$) liquid junction contact in a photoelectrochemical cell. Initial photoelectrochemical conversion efficiencies suggest that the material quality of these microwire arrays is similar to smaller ($\sim$1 cm^2) wire arrays that we have grown in the past, indicating that this technique is a viable way to scale up microwire-array devices.**

***Index Terms*—Microwire, nanowire, photoelectrochemical, photovoltaic.**

I. Introduction

SILICON microwire and nanowire arrays have recently demonstrated their potential for low-cost, high-efficiency photovoltaics [1]–[6] and photoelectrochemical fuel generation [7]–[9]. These high-aspect ratio, radial junction wire arrays allow for the absorption of nearly all the incident sunlight while enabling efficient carrier extraction in the radial direction [10], even in low-quality materials with relatively short minority carrier diffusion lengths [11]. These wire arrays can be embedded in a polymer and removed from the substrate, yielding lightweight, flexible solar cells, while preserving the relatively expensive growth substrate for reuse [12]. We have recently demonstrated single-wire solar cells with open-circuit voltages up to 600 mV [2], 0.1 mm^2 wire-array solar cells with 8% efficiency [1], and photoelectrochemical hydrogen generation with 5% efficiency [7] using these wire arrays. One of the remaining challenges to bringing this technology to the market is growth of microwire arrays over commercially relevant device areas. While there have been numerous reports of nanowire and microwire devices, there have been few reports on wafer-scale fabrication of nanowire or microwire arrays using bottom-up techniques such as vapor–liquid–solid (VLS) growth [13]–[15]. Here, we present a technique for epitaxial growth of silicon microwire arrays covering full six inch wafers.

II. Experimental Methods

Silicon wire arrays are fabricated using vapor-liquid-solid (VLS) chemical vapor deposition (CVD) growth with a Cu catalyst [16]. We favored Cu because it is anticipated to be the best-tolerated impurity for photovoltaic devices [16], although several other catalyst metals are compatible with VLS growth (e.g., Au). Si (111) wafers are prepared with a thermal oxide and then are photolithographically patterned with a hexagonal array of 3 μm holes on a 7 μm pitch. The oxide is then etched, and Cu is deposited into the holes, in contact with the underlying Si. The samples are then heated to 1000 °C in a CVD reactor under hydrogen, and silicon tetrachloride is flowed across the sample at atmospheric pressure, inducing vertical microwire growth. Previously, our microwires were grown in a hot-wall, one-inch diameter tube furnace, leading to a maximum sample size of about 1 cm^2. In addition, hot wall growth induces silicon deposition along the tube walls and $SiCl_4$ depletion along the direction of gas flow, leading to a growth process that is often unpredictable and unsuitable for large area growth.

Our technique for wafer-scale VLS growth uses a cold-wall process with RF heating of a graphite susceptor in a rectangular quartz tube. A single six inch growth wafer sits flat on the susceptor, with gas flow across its top surface as shown in Fig. 1. A typical growth consists of a 5-min ramp at 1000 °C under H_2, a H_2 anneal for 10 min at 1000 °C, and 10–30 min of growth, depending on the desired wire length, with gas flow rates as follows: 10 slm H_2, 2 slm H_2 through the $SiCl_4$ bubbler at room temperature, and a variable flow ($\sim$100 sccm) of BCl_3 for p-type doping, diluted to 5% in H_2. Typical growth rates are about

Manuscript received July 11, 2011; revised March 7, 2012; accepted March 19, 2012. This work was supported in part by the Defense Advanced Research Projects Agency under Contract W911NF-09-2-0011 and in part by the U.S. Department of Energy under Grant DE-FG02-05ER15754.

A. C. Tamboli was with the Department of Applied Physics, California Institute of Technology, Pasadena, CA 91125 USA. She is now with the Department of Physics, Colorado School of Mines, Golden, CO 80401 USA (e-mail: atamboli@mines.edu).

C. T. Chen, D. B. Turner-Evans, and H. A. Atwater are with the Department of Applied Physics, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: chris.t.chen@caltech.edu; dt@caltech.edu; haa@caltech.edu).

M. D. Kelzenberg was with the Department of Applied Physics, California Institute of Technology, Pasadena, CA 91125 USA. He is now with Caelux, Pasadena, CA 91103 USA (e-mail: kelzenbe@caltech.edu).

E. L. Warren and N. S. Lewis are with the Division of Chemistry and Chemical Engineering, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: ewarren@caltech.edu; nslewis@caltech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JPHOTOV.2012.2191941

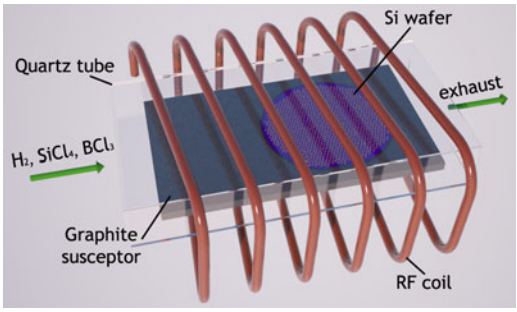

Fig. 1. Diagram of the reactor used for large-area microwire array growth.

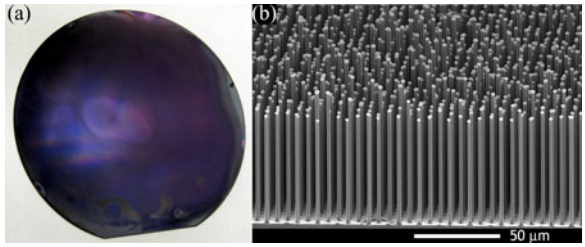

Fig. 2. Photograph of a six-inch wafer covered in Si microwires (left) and SEM image of these wires (right). The wafer was cleaved to enable imaging of wires near its center.

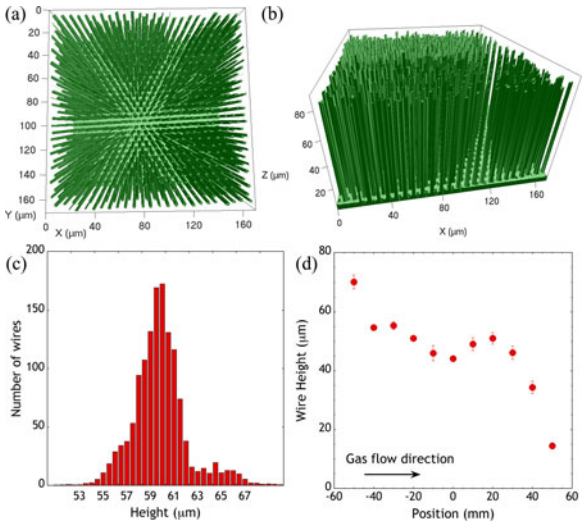

Fig. 3. Confocal microscopy of microwire arrays. (a) and (b) Two different angles of view of the same scan area. (c) Histogram showing distribution of wire heights in a typical wire array section 170 × 170 μm in area. The average height in this case is 59.7 μm, with a standard deviation of 1.4 μm. (d) Wire height for different locations along a wafer, with gas flow during growth indicated by an arrow. Height values represent averages, and error bars represent standard deviations calculated from histograms such as that shown in image (c) over 170 × 170 μm areas.

3–5 μm/min, depending on the precise growth conditions. Growth samples are cooled to 700 °C under H_2 over the course of 15 min so that any Cu in the wires diffuses to the surface, where it can later be removed by a chemical etch. Sample loading and unloading occurs at room temperature.

The energy-conversion properties of these microwire arrays were tested using a liquid junction contact to measure external quantum efficiency, as discussed in [17]. This technique allows us to rapidly evaluate relative material quality in wire arrays as it relates to photovoltaic efficiency, since the liquid junction forms a Schottky junction with p-type Si wires. Samples with areas of 0.05–0.1 cm^2 were cleaved from several wafers, and a partial polymer infill (PDMS) was performed on some pieces to minimize shunting through the wire base and the heavily doped substrate [8]. The photoelectrochemical performance of the arrays was evaluated using a methyl viologen redox couple under 808 nm illumination. Electrodes were fabricated by contacting the back of each sample with Ga/In eutectic and sealing with epoxy. Electrochemistry was performed using 50 mM of $MV^{2+/+}$ in a pH 2.9 phthalate buffer with 0.5 M of K_2SO_4 as a supporting electrolyte.

III. Results

Because of the cold-wall nature of this growth procedure, Si is deposited only on the wafer and susceptor, leading to reduced $SiCl_4$ depletion between the front and back edges of the wafer, and thus to more uniform growth across larger areas. Additionally, the growth conditions are more stable from run to run, since the quartz process tube does not become coated with Si, which would change the gas flow and heating dynamics. In this way, we have been able to grow Si microwires over full six inch wafers, as shown in Fig. 2. A typical growth has a cycle time of less than 1 h from loading to unloading and produces ∼100 μm-long wires with a 30-min growth phase. This growth technique is reliable and reproducible: At the laboratory scale, we have produced more than a square meter of wire array material to date, demonstrating the potential applicability of this technology for photovoltaic manufacturing.

A. Structural Characterization

Microwire arrays were characterized using scanning electron microscopy (SEM) and confocal microscopy to determine their structural quality, including wire fidelity, height, and variation across each wafer. A typical wire array sample is shown in cross-sectional SEM in Fig. 2. As this image shows, the wires are vertically oriented with a very high fidelity, and the wire height is fairly uniform over the area pictured. Confocal microscopy was also used to study wire array geometry, as it allows for rapid screening of arbitrary points on a large wafer, without requiring the wafer to be cleaved. Topography maps were formed by reflective laser-scanning confocal microscopy using 488 nm illumination through a 50× objective with a numerical aperture of 0.95, enabling lateral feature resolution of ∼350 nm. This technique allows the arrays to be visualized as a 3-D model using software. Typical confocal microscope images of a wire array are shown in Fig. 3(a) and (b), which display the same image from two different perspectives. Fig. 3(c) shows a histogram of wire heights, in microns, over the scanned area shown in the images (170 × 170 μm). Wire heights were mapped across the wafer area by acquiring similar images and histograms at preset locations. Fig. 3(d) shows a plot of average wire heights, which is measured over 170 × 170 μm regions, as a function of distance along a wafer from front to back with regard to the gas flow

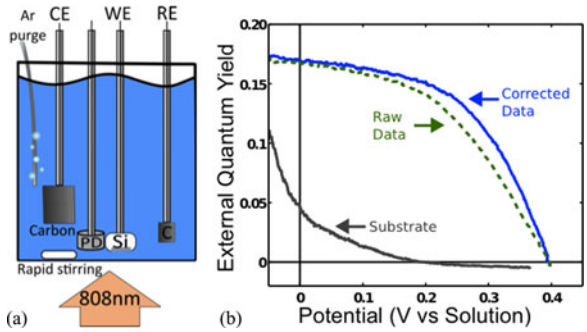

Fig. 4. (a) Schematic of a photoelectrochemical testing setup for wire array electrodes. The counter electrode (CE), working electrode (WE), and reference electrode (RE) are labeled. (b) External quantum yield versus solution potential for an electrode partially embedded in PDMS to prevent shunting. The curve is shown before and after correcting for resistance losses in the solution. Also shown (gray) is the electrochemical performance of the same electrode with the wires scraped off, showing the minimal contribution of the substrate.

direction during growth. These points were taken along the center line of the wafer. This graph shows that wire height varies with spatial location on this wafer, with the fastest growth occurring on the front end of the wafer and the slowest growth near the back edge. This effect is caused by depletion of $SiCl_4$ as silicon is deposited on the wafer and susceptor, and could be minimized by proper choice of susceptor angle, wafer rotation, or modifications to the gas injection, although these variables have not been investigated in this study. There is a slight dip in wire height at the center of the wafer, which is observed in small samples as well, and is caused by increased $SiCl_4$ availability near the edges compared with in the center, where it is locally depleted by nearby Cu reservoirs. Wire height also varies slightly within a given region on the wafer, and this height variation is larger for these samples than for smaller samples because it is more difficult to maintain uniform photolithography over a full wafer than over a small piece of material, resulting in nonuniform Cu droplet size. This nonuniform Cu size results in wires with slightly varying diameters, and thus different growth rates. Better standardization could be achieved using commercial rather than research grade photolithography equipment.

B. Photoelectrochemical Characterization

The external quantum yield under 60 mW cm^{-2} monochromatic 808 nm illumination is plotted as a function of electrode potential for a typical wire array photoelectrode in contact with methyl viologen (see Fig. 4). This illumination intensity was chosen because it provides similar above-bandgap photon flux to the AM 1.5G solar spectrum, which could not be simulated due to strong electrolyte absorption at other wavelengths. The curves show EQY for the same electrode before and after correcting for resistance losses in the solution. Also shown is the EQY curve for the same electrode after the wires have been scraped off, showing the negligible contribution from the heavily doped substrate. The energy-conversion properties of the wire array are good, with a high open-circuit voltage of 400 mV and an overall efficiency of 2.3% in this geometry, which is only slightly lower than the best devices that we reported previously ([17], 3.6% efficiency). Wire arrays similar to those yielding 3.6% efficiency previously reported [17] in these Schottky-junction-based photoelectrochemical measurements have been used to fabricate solid-state photovoltaic devices with efficiencies of 8% [1]. The main reason for the discrepancy between the current samples and those measured previously is doping. Single-wire four-point *I–V* measurements indicated that these wires are doped at 2×10^{18} cm^{-3} (p-type), which is sufficiently high to cause dopant-induced lifetime degradation and thus limit wire performance.

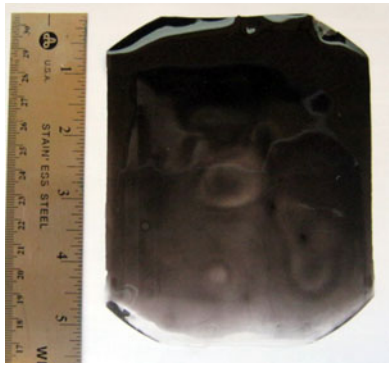

Fig. 5. Photograph of a polymer-embedded microwire array.

C. Removal From the Substrate

We have developed a technique to embed these wafer-scale arrays of wires in polymer and peel them off the substrate, indicating that this aspect of the technology can also be scaled up. PDMS is spun onto the wire arrays using a previously established process [12]. Wafers are then transferred into a home-built peel-off tool, which consists of a vacuum chuck stage and a motorized, spring-loaded razor blade spanning the length of the wafer, which travels along the surface of the wafer to sever the wire/PDMS composite from the substrate. The wafer is left with the patterned oxide intact, and can be reused for wire growth after chemical cleaning and electroplating copper into the holes [12]. Fig. 5 shows a photograph of a polymer-embedded microwire array after it has been removed from the substrate.

IV. Conclusion

In conclusion, we have scaled up the growth of Si microwire arrays to six inch wafers using the VLS technique. These wire arrays maintain the structural quality of previously reported wire arrays grown on a smaller scale, and have suitable fidelity for photovoltaic applications. These wires also demonstrate good energy-conversion properties under photoelectrochemical testing, further illustrating the viability of microwire-array solar cells as a future photovoltaic technology.

Acknowledgments

The authors would like to thank A. Leenheer for assistance with confocal microscopy measurements. Facilities for wafer preparation were provided by the Kavli Nanoscience Institute

at Caltech. D. B. Turner-Evans acknowledges support from a National Science Foundation graduate fellowship.

REFERENCES

[1] M. C. Putnam, S. W. Boettcher, M. D. Kelzenberg, D. B. Turner-Evans, J. M. Spurgeon, E. L. Warren, R. M. Briggs, N. S. Lewis, and H. A. Atwater, "Si microwire-array solar cells," *Energy Environ. Sci*., vol. 3, pp. 1037–1041, 2010.

[2] M. D. Kelzenberg, D. B. Turner-Evans, M. C. Putnam, S. W. Boettcher, R. M. Briggs, J. Y. Baek, N. S. Lewis, and H. A. Atwater, "High performance Si microwire photovoltaics," *Energy Environ. Sci*., vol. 4, pp. 866–871, 2011.

[3] C. E. Kendrick, H. P. Yoon, Y. A. Yuwen, G. D. Barber, H. T. Shen, T. E. Mallouk, E. C. Dickey, T. S. Mayer, and J. M. Redwing, "Radial junction silicon wire array solar cells fabricated by gold-catalyzed vapor-liquid-solid growth," *Appl. Phys. Lett*., vol. 97, p. 143108, 2010.

[4] L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand, "Silicon nanowire solar cells," *Appl. Phys. Lett*., vol. 91, pp. 233117-1–233117-3, 2007.

[5] E. C. Garnett and P. D. Yang, "Silicon nanowire radial p-n junction solar cells," *J. Amer. Chem. Soc*., vol. 130, pp. 9224–9225, 2008.

[6] J.-Y. Jung, Z. Guo, S.-W. Jee, H.-D. Um, K.-T. Park, M. S. Hyun, J. M. Yang, and J.-H. Lee, "A waferscale Si wire solar cell using radial and bulk p-n junctions," *Nanotechnology*, vol. 21, p. 445303, 2010.

[7] S. W. Boettcher, E. L. Warren, M. C. Putnam, E. A. Santori, D. B. Turner-Evans, M. D. Kelzenberg, M. G. Walter, J. R. McKone, B. S. Brunschwig, H. A. Atwater, and N. S. Lewis, "Photoelectrochemical hydrogen evolution using Si microwire arrays," *J. Amer. Chem. Soc*., vol. 133, pp. 1216–1219, 2011.

[8] E. L. Warren, S. W. Boettcher, M. G. Walter, H. A. Atwater, and N. S. Lewis, "pH-independent, 520 mV open-circuit voltages of Si/Methyl Viologen$^{2+/+}$ contacts through use of radial n^+ p-Si junction microwire array photoelectrodes," *J. Phys. Chem. C*, vol. 115, pp. 594–598, 2011.

[9] A. P. Goodey, S. M. Eichfeld, K.-K. Lew, J. M. Redwing, and T. E. Mallouk, "Silicon nanowire array photoelectrochemical cells," *J. Amer. Chem. Soc*., vol. 129, pp. 12344–12345, 2007.

[10] M. D. Kelzenberg, S. W. Boettcher, J. A. Petykiewicz, D. B. Turner-Evans, M. C. Putnam, E. L. Warren, J. M. Spurgeon, R. M. Briggs, N. S. Lewis, and H. A. Atwater, "Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications," *Nat. Mater.*, vol. 9, pp. 239–244, 2010.

[11] B. M. Kayes, H. A. Atwater, and N. S. Lewis, "Comparison of the device physics principles of planar and radial *p-n* junction nanorod solar cells," *J. Appl. Phys*., vol. 97, pp. 114302-1–114302-11, 2005.

[12] J. M. Spurgeon, K. E. Plass, B. M. Kayes, B. S. Brunschwig, H. A. Atwater, and N. S. Lewis, "Repeated epitaxial growth and transfer of arrays of patterned, vertically aligned, crystalline Si wires from a single Si(111) substrate," *Appl. Phys. Lett*., vol. 93, p. 032112, 2008.

[13] M. Cantoro, G. Wang, H. C. Lin, A. V. Klekachev, O. Richard, H. Bender, T.-G. Kim, F. Clemente, C. Adelmann, M. H. van der Veen, G. Brammertz, S. Degroote, M. Leys, M. Caymax, M. M. Heyns, and S. De Gendt, "Large-area, catalyst-free heteroepitaxy of InAs nanowires on Si by MOVPE," *Phys. Status Solidi (a)*, vol. 208, pp. 129–135, 2011.

[14] L. E. Greene, M. Law, J. Goldberger, F. Kim, J. C. Johnson, Y. Zhang, R. J. Saykally, and P. D. Yang, "Low-temperature wafer-scale production of ZnO nanowire arrays," *Angewandte Chem*., vol. 42, pp. 3031–3034, 2003.

[15] Y. Wei, W. Wu, R. Guo, D. Yuan, S. Das, and Z. L. Wang, "Wafer-scale high throughput ordered growth of vertically aligned ZnO nanowire arrays," *Nano Lett*., vol. 10, pp. 3414–3419, 2010.

[16] B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, and H. A. Atwater, "Growth of vertically aligned Si wire arrays over large areas (>1 cm^2) with Au and Cu catalysts," *Appl. Phys. Lett*., vol. 91, p. 103110, 2007.

[17] S. W. Boettcher, J. M. Spurgeon, M. C. Putnam, E. L. Warren, D. B. Turner-Evans, M. D. Kelzenberg, J. R. Maiolo, H. A. Atwater, and N. S. Lewis, "Energy-conversion properties of vapor-liquid-solid-grown silicon wire-array photocathodes," *Science*, vol. 327, pp. 185–187, 2010.

Authors' photographs and biographies not available at the time of publication.