RADIAL PN JUNCTION, WIRE ARRAY SOLAR CELLS

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ABSTRACT

Radial pn junctions are of interest in photovoltaics because of their potential to reduce the materials costs associated with cell fabrication. However, devices fabricated to date based on Au-catalyzed vapor-liquid-solid growth have suffered from low open-circuit voltages (to our knowledge the highest reports are 260 mV in the solid state and 389 mV in solid-liquid junctions). Herein we report on the potential of low-cost catalysts such as Cu and Ni to fabricate Si wire arrays with potentially higher minority-carrier lifetimes than is possible with a Au catalyst, as well as on the use of reactive ion etching to fabricate high-purity analogs to vapor-liquid-solid grown arrays.

INTRODUCTION

We have previously reported on the potential of radial pn junction wire array solar cells, that is, cells which consist of a dense array of semiconducting wires where each wire has a pn junction in the radial direction (Fig. 1), to reduce the materials costs associated with photovoltaic (PV) device fabrication [1,2]. Recently, PV devices based on Si nanowires with radial pn junctions have been demonstrated experimentally, both at the single-wire [3], and at the large-area [4] level. Also, semiconductor-liquid junctions based on large-area wire arrays have been reported [5,6]. In all cases, the wires were grown by the vapor-liquid-solid (VLS) process [7], using Au as the catalyst. While these results are impressive, the open-circuit voltages (V_{oc}s) reported in each case (up to 260 mV, 130 mV, 389 mV, and 230 mV respectively) are relatively low for Si devices, possibly implying a trap density near the junction that is too high to allow for high-quality devices. It would therefore be desirable to explore the geometrical effects on photovoltage of the radial pn junction geometry independent of the effects of catalyst incorporation, as well as to explore the fabrication of wire arrays with catalysts less injurious to the properties of Si than Au is.

Here we report on the fabrication of large area wire arrays using Ni and Cu catalysts that may be less detrimental to the PV properties of Si than Au is. We also report on the solid state characterization of reactive ion etched (RIE) wire arrays that serve as a model analog to grown wire arrays, and provide insight into the effects of morphology on device performance without convolution with the effects of catalyst incorporation.

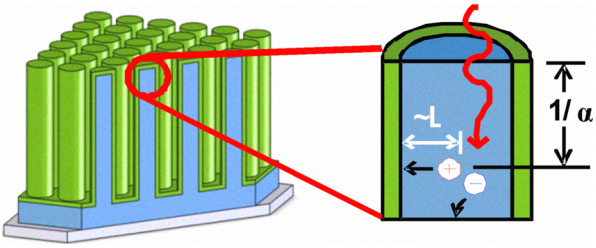

Fig. 1. Schematic and cross-section of the radial pn junction wire array cell. Light is incident on the top surface. The pn junction follows the contours of the high-aspect ratio wires, allowing for a cell that is optically thick (thickness > ~ 1/α, where α is the absorption coefficient of the material), while ensuring that all minority carriers are less than a diffusion length (L) from the junction.

BACKGROUND

A key conclusion of our previous theoretical work [2] was that the radial pn junction geometry can accommodate practically arbitrarily low minority carrier diffusion lengths in the case where quasi-neutral region recombination is dominant over depletion region recombination (i.e. recombination at the junction itself). This is because current collection can remain high by tuning the wire radius to be less than a minority carrier diffusion length while voltage drops only rather mildly with increasing aspect ratio in this regime (~59 mV per factor of 10 increase in junction area at 25 °C [8]). As trap density increases so that minority carrier diffusion lengths decrease, this condition requires that the trap density in the depletion region remain fixed at a level that prevents depletion region recombination from dominating. However, if depletion region trap density is set equal to the quasi-neutral region trap density and overall trap density is increased, our previous work predicts that there is a critical trap density and wire aspect ratio at which depletion region recombination begins to dominate. As trap density and/or aspect ratio is increased beyond this value, V_{oc} drops much more rapidly. Our previous work predicted that this transition occurs for Si at quasi-neutral region diffusion lengths of ~10 μm, or, equivalently, lifetimes of ~100 ns, or, assuming the trapping characteristic of Au impurities, a trap density of ~10^{15} cm^{-3}. This potentially limits the effectiveness of the radial pn junction geometry in that it may set a lower limit on material quality, albeit a more forgiving one than is set by a

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planar geometry in the absence of very effective light trapping.

We have previously reported on a technique for the fabrication of high-fidelity arrays of Si wires with diameters of 2-3 μm and lengths of up to hundreds of μm [9]. We have also reported on the single-wire optoelectronic [10] and chemical [11] characterization of these wires. One conclusion of the former work was that minority hole diffusion lengths are ~2 μm in as-grown, Au-catalyzed Si wires, grown by VLS with $SiCl_4$ at 1000 °C. This is consistent with the latter work, which saw, by taking secondary ion mass spectra of individual wires, Au concentrations of ~1.6 x 10^{16} cm^{-3} inside the "bulk" of each wire (surface concentrations were higher). This is also consistent with the notion that the vapor-liquid-solid (VLS) catalyst is being incorporated into the growing crystal at its solubility limit at the growth temperature [12], at least for wires of the size scale considered here, and under our growth conditions.

As stated above, we expect that Au concentrations this high will lead to degradation of V_{oc} in addition to purely geometrical effects, and therefore additional loss in overall device performance. The use of alternative catalysts may allow for the VLS growth of higher-quality Si than is possible with a Au catalyst. The bulk solubility of Cu and Ni at our growth temperature (1000 °C) have been reported as ~3 x 10^{17} cm^{-3} and ~1 x 10^{17} cm^{-3}, respectively [12,13], which for the case of Cu at least is slightly below the concentration at which impurities have been seen to degrade solar cell performance [14]. Also, both elements are far more diffusive in Si than is Au [15], which lends them possibly to be more easily gettered [16]. Finally, Si with large diffusion lengths (> 30 μm) has been grown directly from a Si-Cu melt by liquid phase epitaxy at temperatures similar to our growth temperatures, and high-performance PV devices fabricated from this material [17]. However, both Ni and Cu can both form silicides with Si which can potentially significantly degrade material quality [18], and so stricter processing control may be required in attempting VLS growth with these catalysts.

EXPERIMENTAL

High-fidelity wire arrays were grown from evaporated Cu (Fig. 2a) and Ni (Fig. 2b) catalysts by a method described previously [9]. As previously reported, wire arrays were grown by photolithographically patterning S1813 photoresist on an oxide covered Si(111) wafer, then exposing it for 4 min to buffered HF, followed by thermal evaporation of 300 nm of Cu or Ni and lift-off of the resist. The oxide buffer layer was found to be critical to isolate the regions of metal catalyst and prevent ripening during the early stages of the VLS growth process. During Ni evaporation, a low temperature sample stage was required to prevent strain in the Ni film from damaging the photoresist film. This procedure produced a square array of 3 μm diameter catalyst islands with a center-to-center distance of 7 μm, as defined by the photolithography.

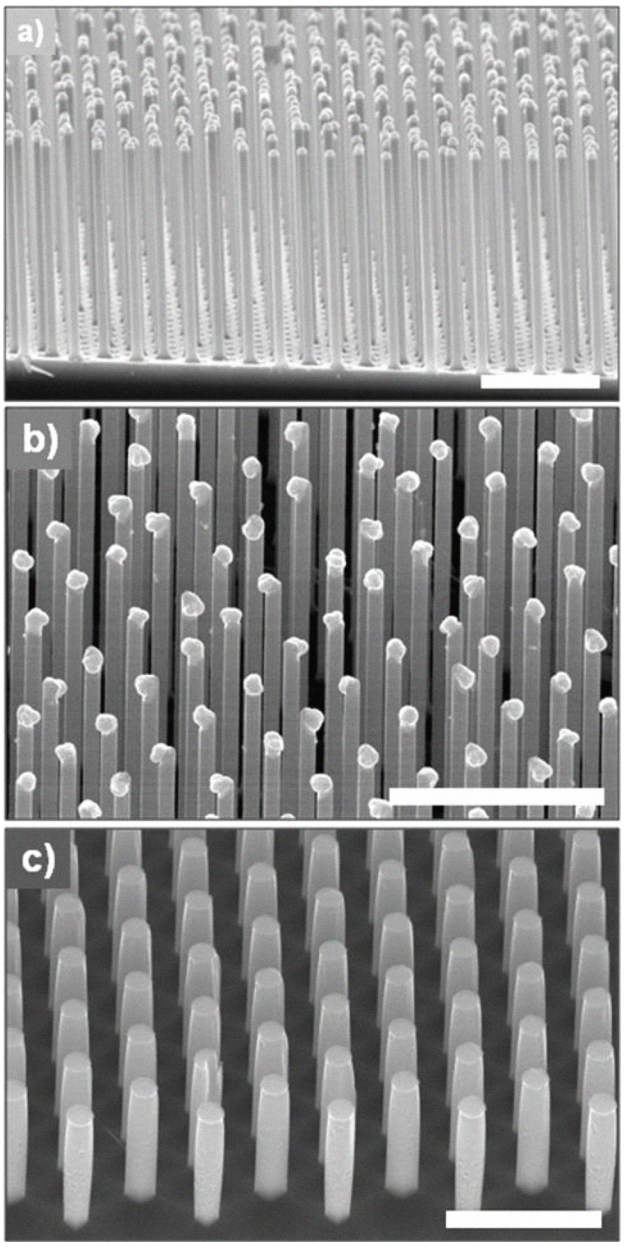

Fig. 2. Examples of Si wire arrays fabrication (a) by VLS, using a Cu catalyst, (b) by VLS, using a Ni catalyst, and (c) by RIE. The scale bar is 20 μm in each case.

Samples were then annealed in a tube furnace at 1000 °C for 20 min under H_2 at a flow rate of 1000 sccm, followed by wire growth at the same temperature under H_2 and $SiCl_4$, at flow rates of 1000 and 20 sccm, respectively. All of this was done at atmospheric pressure. The resulting material consisted of vertically oriented, crystalline Si wires that were 1.5 – 2.0 μm in diameter, greater than 70 μm in

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length, and spaced on the substrate with a 7 μm center-to-center pitch.

To date, efforts to fabricate solid-state PV devices from Cu- and Ni-catalyzed wire arrays have suffered from fabrication difficulties, primarily associated with macroscopic shunting. However, we see no fundamental barrier to achieving this, and this will be the subject of a future publication. In order to more easily fabricate devices, as well as to probe the geometrical effects associated with this device design free from the convoluting effects of catalyst incorporation, we have pursued RIE [19] as a means to fabricate analogous wire arrays.

N-type, P-doped Si(100) wafers of 2-8 Ω cm resistivity were first cleaned in acetone, isopropanol, and methanol, followed by a deionized (18 MΩ cm) (DI) H_2O rinse. Wafers were then soaked in buffered HF acid for 2 mins and then dried in an oven at 125 °C for 10 mins. Samples were spin-coated with AZ-5214E photoresist at 6000 RPM, baked at 95 °C, and patterned photolithographically, followed by another 95 °C bake. These patterned samples were then introduced to a plasma-enhanced chemical vapor deposition (PECVD) chamber for deposition of an SiO_2 etch mask. The oxide was deposited at a temperature T = 135 °C for 9-10 mins at a SiH_4 flow rate of 450 sccm, N_2O flow rate of 750 sccm, a total pressure P of 1 Torr, and an RF power of 15 W, leading to an SiO_2 deposition rate of ~ 65 nm/min. Si etching was then performed using a SF_6 etchant. This was done at T = -110 °C, SF_6 flow rate of 70 sccm, O_2 flow rate of 6 sccm, and P = 10 mTorr. The inductively coupled plasma (ICP) power was 900 W at 56 MHz, with a forward power of 8W, leading to an etch rate of 1.9-2.0 μm/min. The etching was done in 15 min increments with 10 min pumpdown in between, in order to prevent trapping of the etchant gas and/or reaction products within the bottoms of the etched structures.

In this way, wire arrays of a fixed packing fraction of 22.7% were fabricated. Four different wire diameters, 5 μm, 10 μm, 20 μm, and 50 μm, were considered, with pitch equal to twice the wire diameter, in a close-packed hexagonal arrangement. After array fabrication, samples were etched for 1 hour in piranha solution (3:1 H_2SO_4:H_2O_2 by volume) at room temperature, in order to remove bonding grease used for sample mounting in the RIE process. Any oxide was then removed in buffered HF. Sample were then oxidized at 850 °C for 1.5 hours in N_2 bubbled through near-boiling, DI H_2O at 3 liters per minute (lpm) flow rate. Oxide on the front (device) surface was then removed with buffered HF. Samples were then annealed at 400 °C for 30 mins, under forming gas (5% H_2 in N_2%) at 5 lpm. The front surface of the samples were then doped p-type by stacking parallel to BN diffusion wafers (BN-975, Saint-Gobain Ceramics), introducing to a tube furnace at 750 °C, ramping up to 950 °C, holding at 950 °C for 40 mins, and then ramping back down, all under N_2 at 5 lpm. The front surface was then exposed to buffered HF for 2 mins. This was followed by a low temperature

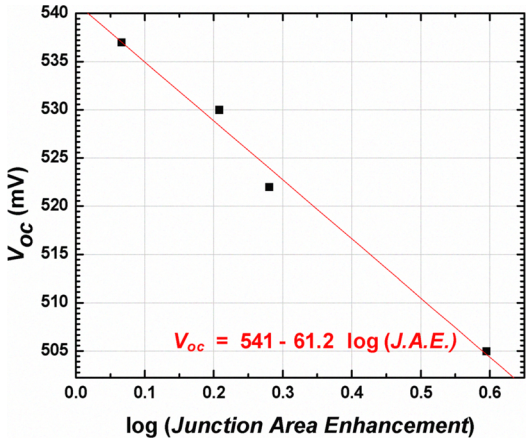

Fig. 3. Effect of increased junction area on V_{oc}. In this case we see a 61 mV loss of V_{oc} per decade increase in junction area, close to the 59 mV decrease per decade that we expect in the quasi-neutral region recombination-dominated regime.

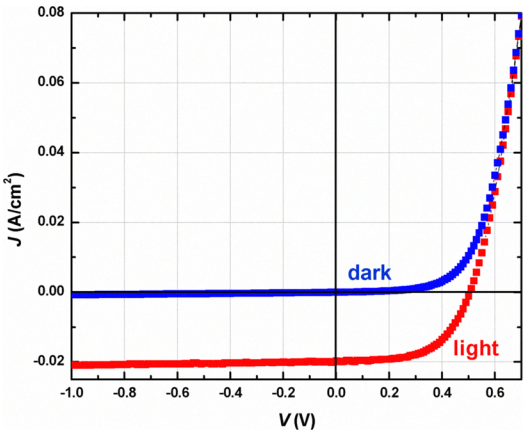

Fig. 4. *J-V* curve for measured 5 μm-diameter wire array. Efficiency = 5.7%, V_{oc} = 505 mV, J_{sc} = 19.7 mA/cm^2, *FF* = 57.7 %, total cell area 12.9 mm^2, wire array area 4 mm^2.

oxidation at 750 °C for 20 mins, under O_2 at 5 lpm. Finally, oxide was removed from the entirety of the samples with buffered HF, and contact was made to the back surface by immediately rubbing Ga/In onto the back of the sample and the sample then bonded with Ag paste to a piece of stainless steel to which electrical contact could be made with a probe tip. Contact was made to the front surface with a spot of Ga/In and an electrical probe tip.

Samples were then tested in the light (under AM1.5D sunlight at 1 sun intensity, as calibrated with a BP Solar reference cell) and in the dark. This results in excitation of

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the wire array as well as the underlying Si and the adjoining planar regions. This limited our ability to increase the junction area to only a factor of ~4. Nevertheless, initial results indicate a loss of V_{oc} of approximately 61 mV per factor of ten increase in junction area (Fig. 3), as well as a decrease in fill factor (*FF*) as junction area increases. To verify that the wires were indeed contributing photocurrent to the device, we performed scanning photocurrent measurements using an excitation wavelength of 650 nm (which has an absorption depth $1/\alpha$ of ~3 μm), which showed that comparable photocurrent was generated in the wires and in the planar substrate (not shown). In the best device, with 50 μm diameter wires, we observed an efficiency of 6.7%, with V_{oc} = 537 mV, J_{sc} = 18.8 mA/cm^2, and *FF* = 66.1% (not shown). For this sample, the total cell area was 22.9 mm^2 with a wire array area of 4 mm^2. In all cases, J_{sc} was calculated by normalizing to the total cell area. Even in the case of relatively small wires of 5 μm diameter, occupying a larger fraction of the sample (total cell area 12.9 mm^2, wire array area 4 mm^2), we saw an efficiency of > 5% and V_{oc} > 500 mV (Fig. 4).

CONCLUSIONS

Radial pn junction wire arrays are a novel approach to the creation of efficient solar cells using low lifetime materials. To attain high efficiency in this new geometry it is essential that the depletion region trap density remain relatively low. For Si with a homogeneous distribution of impurities, we expect that minority carrier lifetimes of > 100 ns will be required. We have demonstrated the growth of high-fidelity VLS-grown Si wire arrays using Cu and Ni as catalysts. This is an important alternative to the more commonly used Au, both from an economic point of view, but also, we expect, in terms of the effect of the catalyst on the optoelectronic properties of the Si. To investigate any purely geometrical limitations to the radial pn junction geometry, we have explored the use of RIE to fabricate analogous PV cells. With these cells we observe a loss in V_{oc} of 61 mV per decade increase in junction area. This supports the notion that losses in V_{oc} associated with purely geometrical effects in the radial pn junction design should be tolerable in the pursuit of efficient devices.

Future efforts will target the characterization of devices wherein the Si absorber layer has been grown by VLS using Cu or Ni as the growth catalyst, as well as substrate-free device measurements exploiting a technique we have developed for removing grown wire arrays from their growth substrates [20].

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REFERENCES

[1] B.M. Kayes et al., "Radial PN Junction Nanorod Solar Cells: Device Physics Principles and Routes to Fabrication in Silicon", *Thirty-first IEEE PVSC*, 2005, pp. 55-58.

[2] B.M. Kayes, H. A. Atwater, and N. S. Lewis, "Comparison of the Device Physics Properties of Planar and Radial p-n Junction Nanorod Solar Cells", *J. Appl. Phys.* **97**, 2005, Art. No. 114302.

[3] B.Z. Tian et al., "Coaxial Silicon Nanowires as Solar Cells and Nanoelectronic Power Sources", *Nature* **449**, 2007, pp. 885-890.

[4] L. Tsakalakos et al., "Silicon Nanowire Solar Cells", *Appl. Phys. Lett.* **91**, 2007, Art. No. 233117.

[5] J.R. Maiolo et al., "High Aspect Ratio Silicon Wire Array Photoelectrochemical Cells", *J. Amer. Chem. Soc.* **129**, 2007, pp. 12346-12347.

[6] A.P. Goodey et al., "Silicon Nanowire Array Photoelectrochemical Cells", *J. Am. Chem. Soc.* **129**, 2007, pp. 12344 -12345.

[7] R.S. Wagner and W.C. Ellis, "Vapor-Liquid-Solid Mechanism of Single Crystal Growth", *Appl. Phys. Lett.* **4**, 1964, pp. 89-90.

[8] J.M. Spurgeon, H.A. Atwater, and N.S. Lewis., "A Comparison Between the Behavior of Nanorod Array and Planar Cd(Se, Te) Photoelectrodes", *J. Phys. Chem. C* **112**, 2008, pp. 6186-6193.

[9] B.M. Kayes, M.A. Filler et al., "Growth of Vertically Aligned Si Wire Arrays Over Large Areas (> 1 cm^2) With Au and Cu Catalysts", *Appl. Phys. Lett.* **91**, 2007, Art. No. 103110.

[10] M.D. Kelzenberg et al., "Photovoltaic Measurements in Single-Nanowire Silicon Solar Cells", *Nano Lett.* **8**, 2008, pp. 710-714.

[11] M.C. Putnam et al., "Secondary Ion Mass Spectrometry of Vapor-Liquid-Solid Grown, Au-Catalyzed, Si Wires", *Nano Lett.* submitted.

[12] J.D. Struthers, "Solubility and Diffusivity of Gold, Iron, and Copper in Silicon", *Jour. App. Phys.* **27**, 1956, p. 1560.

[13] J.H. Aalberts and M.L. Verheijke, "The Solid Solubility of Nickel in Silicon Determined by Neutron Activation Analysis", *App. Phys. Lett.* **1**, 1962, pp. 19-20.

[14] A.A. Istratov and E.R.Weber, "Electrical Properties and Recombination Activity of Copper, Nickel and Cobalt in Silicon", *Appl. Phys. A* **66**, 1998, pp. 123–136.

[15] A. Luque and S. Hegedus, *Handbook of Photovoltaic Science and Engineering*, John Wiley & Sons, 2003, p. 189.

[16] J.S. Kang and D.K. Schroder, "Gettering in Silicon", *J. App. Phys.* **65**, 1989, pp. 2974-2985.

[17] T.F. Ciszek et. al., "Growth of thin crystalline silicon layers for photovoltaic device use", *Jour. Cryst. Growth* **128**, 1993, pp. 314-318.

[18] R. Sachdeva, A.A. Istratov, and E.R. Weber, "Recombination Activity of Copper in Silicon", *App. Phys. Lett.* **79**, 2001, pp. 2937-2939.

[19] M.J. de Boer, "Guidelines for Etching Silicon MEMS Structures Using Fluorine High-Density Plasmas at Cryogenic Temperatures", *Jour. Microelectromech. Sys.* **11**, 2002, pp. 385-401.

[20] K. E. Plass, M.A. Filler, et al., "Fabrication of Flexible Polymer-Embedded Si Wire Arrays", in preparation.

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