

A flexible phased array system with low areal mass density

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Phased arrays are multiple antenna systems capable of forming and steering beams electronically using constructive and destructive interference between sources. They are employed extensively in radar and communication systems but are typically rigid, bulky and heavy, which limits their use in compact or portable devices and systems. Here, we report a scalable phased array system that is both lightweight and flexible. The array architecture consists of a self-monitoring complementary metal-oxide-semiconductor-based integrated circuit, which is responsible for generating multiple independent phase- and amplitude-controlled signal channels, combined with flexible and collapsible radiating structures. The modular platform, which can be collapsed, rolled and folded, is capable of operating standalone or as a subarray in a larger-scale flexible phased array system. To illustrate the capabilities of the approach, we created a 4×4 flexible phased array tile operating at 9.4–10.4 GHz, with a low areal mass density of 0.1 g cm^{-2} . We also created a flexible phased array prototype that is powered by photovoltaic cells and intended for use in a wireless space-based solar power transfer array.

The development of phased arrays that are lightweight, collapsible and foldable could notably extend the applications of such systems beyond their conventional use in radar^{1–10} and communications^{11–19}. A compactly stored self-deployable large-scale phased array could, in particular, provide a new approach to communication, sensing and power transfer spacecraft. Lightweight architectures are, for example, essential for practical and cost-effective space and drone deployment due to the strong dependence of launch cost on mass. Terrestrial applications, such as wearables^{20–22} or rapidly deployable emergency communication networks^{23–25}, also place a premium on mass and flexibility, and the fabric-like qualities of conformal arrays provide a variety of intriguing storage and usage properties that would not be possible with rigid designs^{26–29}.

Key to the fabrication of such arrays is silicon microwave integrated circuit technology. It provides a unique way to incorporate all necessary array functions and features on a low-cost, lightweight and small silicon substrate with high yield and high repeatability. However, this technology alone cannot deliver lightweight and foldable phased arrays, as the mass and inflexibility of even a low-complexity conventional printed circuit board is prohibitive. For example, the areal mass density of a low-complexity four-layer printed circuit board using Rogers 4003 substrate exceeds 0.41 g cm^{-2} . Even theoretical studies of space-based phased arrays with multilayer tiles estimate the areal mass of such arrays to be $\sim 0.6 \text{ g cm}^{-2}$ (ref. ³⁰). In this Article, we report an integrated circuit-based phased array system that is scalable, flexible and collapsible, and has an areal mass density of 0.1 g cm^{-2} .

Large-scale lightweight array

To be of use in a variety of applications, flexible phased arrays (FPAs) require a broad range of output power levels, apertures and

physical dimensions. To meet these requirements, we developed a scalable phased array architecture (Fig. 1) in which arrays of varying sizes can be formed out of identical elements working in concert. These identical elements (tiles) are synchronized to a shared low-frequency reference signal³¹, which improves the signal integrity and lowers the power consumption of the system, as well as relaxing the off-chip design requirements compared to high-frequency reference distribution approaches. The distributed array architecture is more robust to local element or tile failures than a centralized architecture³². Additionally, the distributed nature of power conversion and radiofrequency (RF) signal generation and radiation offers significant advantages from the thermal management perspective, which can eliminate the need for emissive infrared (IR) material³³. The tile's integrated circuit—called the power synthesis and control unit (PSCU)—generates multiple independent phase-controlled high-frequency signals from a low-frequency timing reference. Independently controlled power amplifiers of the PSCU generate RF power based on these signals to drive the off-chip electromagnetic radiators of the array.

Complementary metal-oxide-semiconductor (CMOS) technology has shown significant promise in high-frequency electromagnetically active systems. In particular, it has been used for the integration of phased array functions^{34–36}, the creation of scalable tile-able phased arrays³⁷ using low-frequency reference distribution³¹ and the demonstration of two-dimensional (2D) beam-forming and pattern scanning³⁸. Our PSCU, integrated in a standard CMOS process, performs all the key array functions, eliminating the need for multiple dies and/or bulky discrete components. The PSCU is light, low profile and well suited for compact storage.

Phased arrays with high beam-forming efficiency and large beam-steering range require efficient individual radiators that

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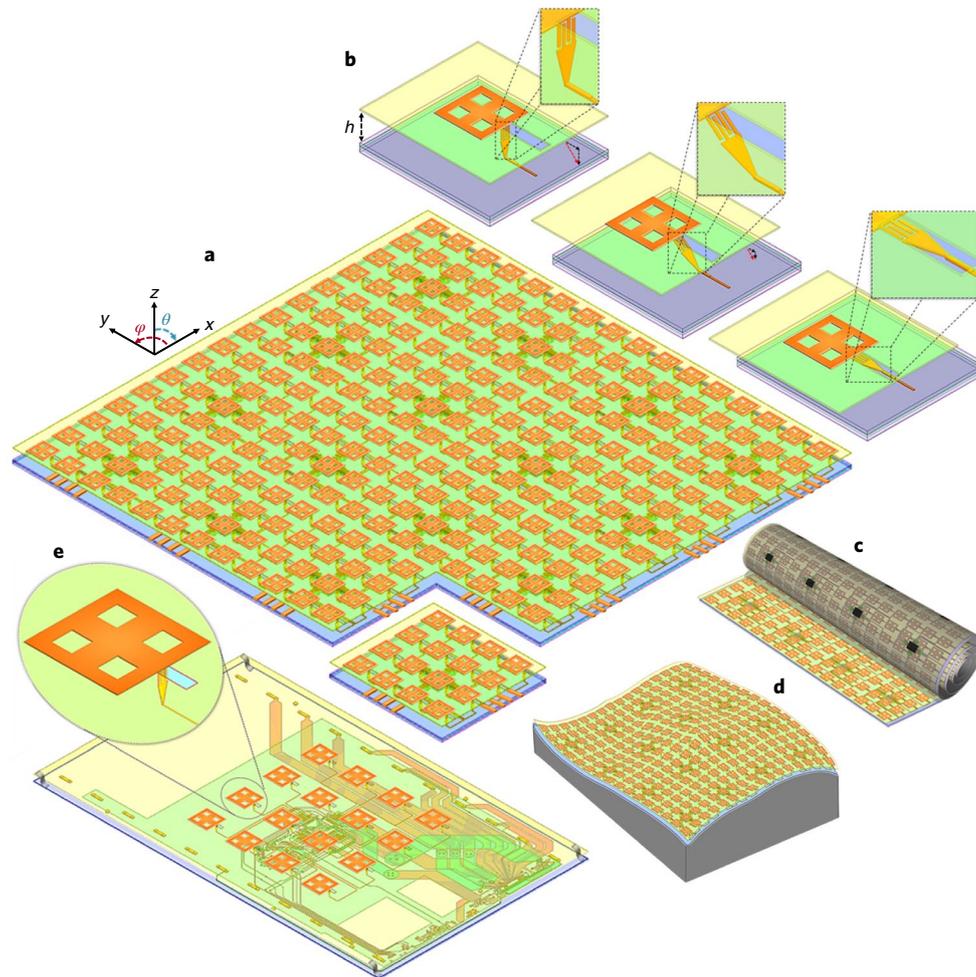


Fig. 1 | Phased array system architecture and its capabilities. **a**, The system uses a scalable and modular design in which arrays of different sizes can be formed from identical elements (or tiles). **b**, The radiators have a collapsing and deploying mechanism in which collapsible and deployable tiles and large-scale arrays can be created. **c**, The resulting phased arrays are rollable and storable. **d**, The resulting phased arrays are flexible and conformable. **e**, The standalone fully operational tile can also be powered by photovoltaic (PV) solar cells.

have broad one-sided beam patterns. Such radiators generally require thickness in the radiation direction. This thickness is usually achieved with dielectric materials, which result in inflexibility and excess mass. Inflatable deployable antennas have been proposed for thin-membrane substrate conformal antennas for terrestrial and space applications^{39–42}. Our self-deployable architecture (Fig. 2) provides the compact storage advantage of inflatable structures due to the air/vacuum gap dielectric, without the added complexities and potential failure modes involved in the inflation phase and pressure control of such systems, especially in space. Each tile consists of a flexible multilayer polyimide circuit board with the PSCU separated by the air gap dielectric from a sheet of radiators created using a single polyimide/conductor layer. During storage, the layers can be collapsed together and rolled compactly.

FPA tile

In a scalable architecture, the tile design plays a central role in the overall performance and behaviour of the FPA, and non-rigidity introduces challenges that must be addressed by the design. We developed a fully functional prototype unit tile for a flexible, foldable, compactible phased array. This proof-of-concept tile has 16 independently controlled radiating elements, all driven by a single PSCU that generates, conditions and amplifies 10 GHz drive signals.

Collapsible and foldable arrays favour low-profile, planar and compact radiating structures. Patch-type antennas⁴³ provide these attributes in a simple form factor. To further reduce the areal mass density of the phased array, the metal patch and the ground plane can be thinned or meshed. We use a fractal inspired modified patch (FIMP) radiator with an air dielectric to obtain a low-profile, collapsible and lightweight radiating element without sacrificing flexibility and performance. This FIMP is inspired by the Sierpinski carpet^{29,44,45}, where the active metal area can be reduced by removing four smaller squares from within the patch, resembling a first-order square fractal antenna^{46–48}. The radiator still operates based on the fringe fields at its two radiating edges with similar performance as a patch, with lower metal mass (Fig. 3a). Each radiator consists of an edge-fed square metallic patch fabricated on a single polyimide/conductor layer placed above another conductive layer on polyimide with an air gap distance of $\lambda_0/10$ chosen. The lower conductor serving as a high-frequency ground plane is part of a multilayer flexible conductor and polyimide board that contains PSCU as well as signal and power distribution lines.

The high-frequency signals are delivered to the FIMP using feedlines, connecting the lower flexible board to the radiating sheet across the air dielectric. To achieve and maintain the collapsibility and high performance of the FPA, the collapsible antenna feedline has to be designed properly from both mechanical and

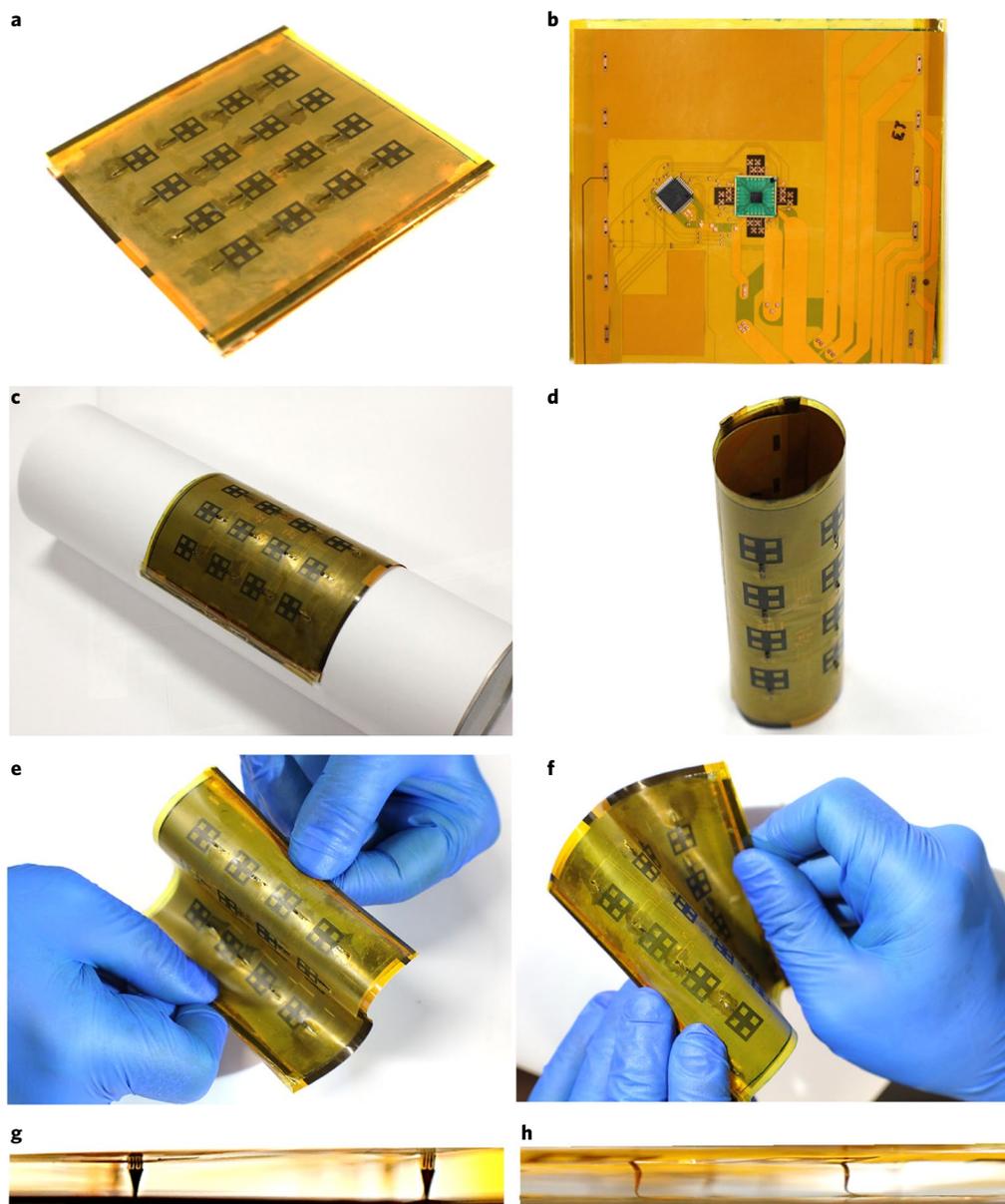


Fig. 2 | Photographs of the proof-of-concept active phased array. a, Radiator layer top view of the tile in a flat deployed state. **b,** Radio frequency integrated circuit (RFIC) side in the flat state. **c,** Array deployed and conformed to a cylindrical object with a radius of 3.2 cm. **d,** Illustration of rollability. **e,** Illustration of flexibility and bending capability. **f,** Illustration of flexibility and twisting capability. **g,h,** Side views of the feedlines configuration and transition between the radiator single flexible layer and the RF flexible four-layer boards in the deployed state.

electromagnetic perspectives. The direction and collapsibility of the feedlines must be consistent across the entire array for reliable rolling and wrapping. As such, feedlines tapping into the radiators must be oriented in the same direction. The FIMP radiators are therefore edge-fed by a collapsible ‘ f ’-shaped feeding transitions (Figs. 1b and 3a). The feed transitions connecting the radiator to the high-frequency transmission lines on the lower multilayer board consist of an interdigital capacitor connected to a tapered section. They provide a resonance impedance match between the radiators and the distribution lines. The capacitive loading of this matching approach also results in a smaller radiator (for example, $9 \times 9 \text{ mm}^2$ at 10 GHz) at the same resonance frequency compared to a conventional half-wavelength patches. Details on the feedline for a 10 GHz FIMP antenna, including the interdigital capacitor value and layout, are provided in the Methods. This collapsible

radiator configuration results in a higher bandwidth due to larger spacing to the ground plane compared to conventional solid dielectric patch antennas, while significantly lowering the mass and stored volume.

The reflection coefficient of the driving port of a single radiator versus frequency is shown in Fig. 3c. The simulated and measured results track closely, showing a reflection coefficient better than -30 dB at the frequency of interest with a bandwidth in excess of 12% with a designed port impedance of 75Ω . The simulated and measured radiation patterns of the radiated electric field along the E plane ($\varphi = 90^\circ$) and H plane ($\varphi = 0^\circ$) are shown in Fig. 3e. The design FIMP antenna has a radiation efficiency of 97% and maximum total gain of 7.88 dBi at the resonance frequency.

Despite their significant mass reduction and collapsibility advantages, these radiators are more prone to shape variations and

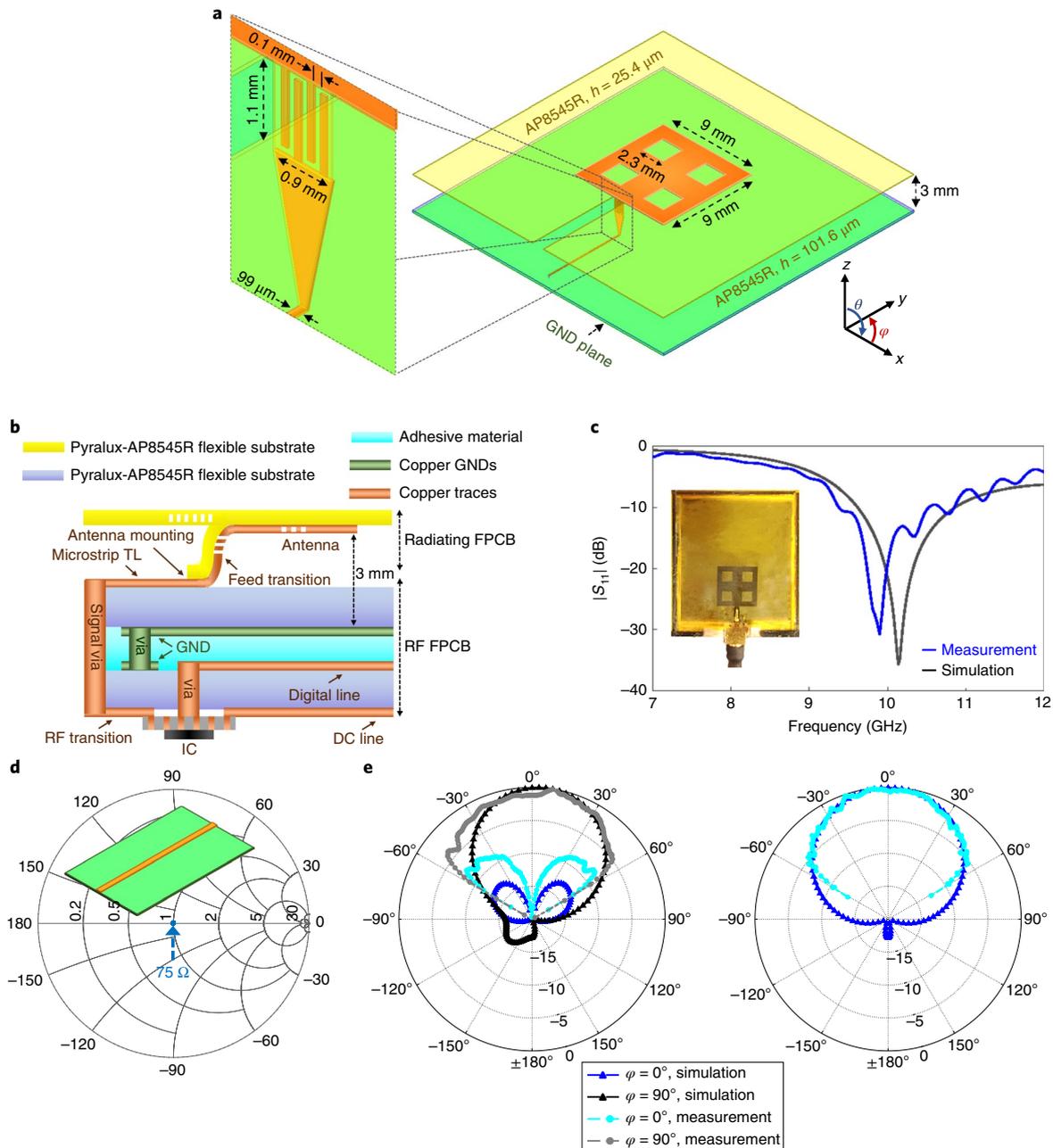


Fig. 3 | Flexible fractal inspired modified patch antenna. **a**, Schematic of the radiator. **b**, Cross-sectional view of the flexible layers stack. **c**, Simulated (black curve) and measured (blue curve) return loss of the flexible radiator. Inset, top view of the working flexible FIMP radiator prototype. **d**, Simulated impedance of the designed $75\ \Omega$ flexible transmission-line. Inset, the transmission-line configuration. **e**, Comparison of simulated and measured radiation patterns along the E plane ($\varphi = 90^\circ$) and H plane ($\varphi = 0^\circ$) for E_θ (left plot) and E_φ (right plot) at the resonance frequency. GND, ground; FPCB, flexible printed circuit board; TL, transmission-line; IC, integrated circuit.

changes, which could be detrimental to high-frequency performance. The sensitivity of the implemented flexible FIMP radiators to shape changes was analysed for a pitch, single- and double-sided bends, and a tilt of the radiator layer, as shown in Supplementary Figs. 11–14, respectively. Of these four deformation scenarios, a forward pitch is most impactful on antenna performance. The centre frequency exhibits a sensitivity of 33.25 MHz per $^\circ$, while the drive port reflection coefficient has a dependency of 2.22 dB per $^\circ$. The radiation efficiency is degraded by 0.043% per $^\circ$ and the radiated beam area varies by 0.027 sr per $^\circ$. Also, the FIMP radiators are insensitive to misalignments, with the centre frequency showing less than 0.133, 0.038, 0.209 and 0.912 GHz of variations over ranges

of 0.099, 2.4, 2.4 and 1 mm of misalignment in the $\pm x$, $-y$, $+y$ and $+z$ directions, as shown in Supplementary Figs. 15–17, respectively. Thus, the presented design is robust to the inevitable shape and dimensional variations in flexible and collapsible systems.

The PSCU is responsible for synthesizing multiple phase- and amplitude-controlled, high-power signals to drive up to 16 radiators. The PSCU of the presented prototype is implemented in a bulk 65 nm CMOS processor and provides 16 independently controlled RF outputs with greater than 360° phase control over a frequency range of 9.4–11 GHz. The PSCU uses four identical quadrants to produce 16 outputs. The top-level circuit block diagrams are shown in Fig. 4d,e (the corresponding equivalent circuits are provided in

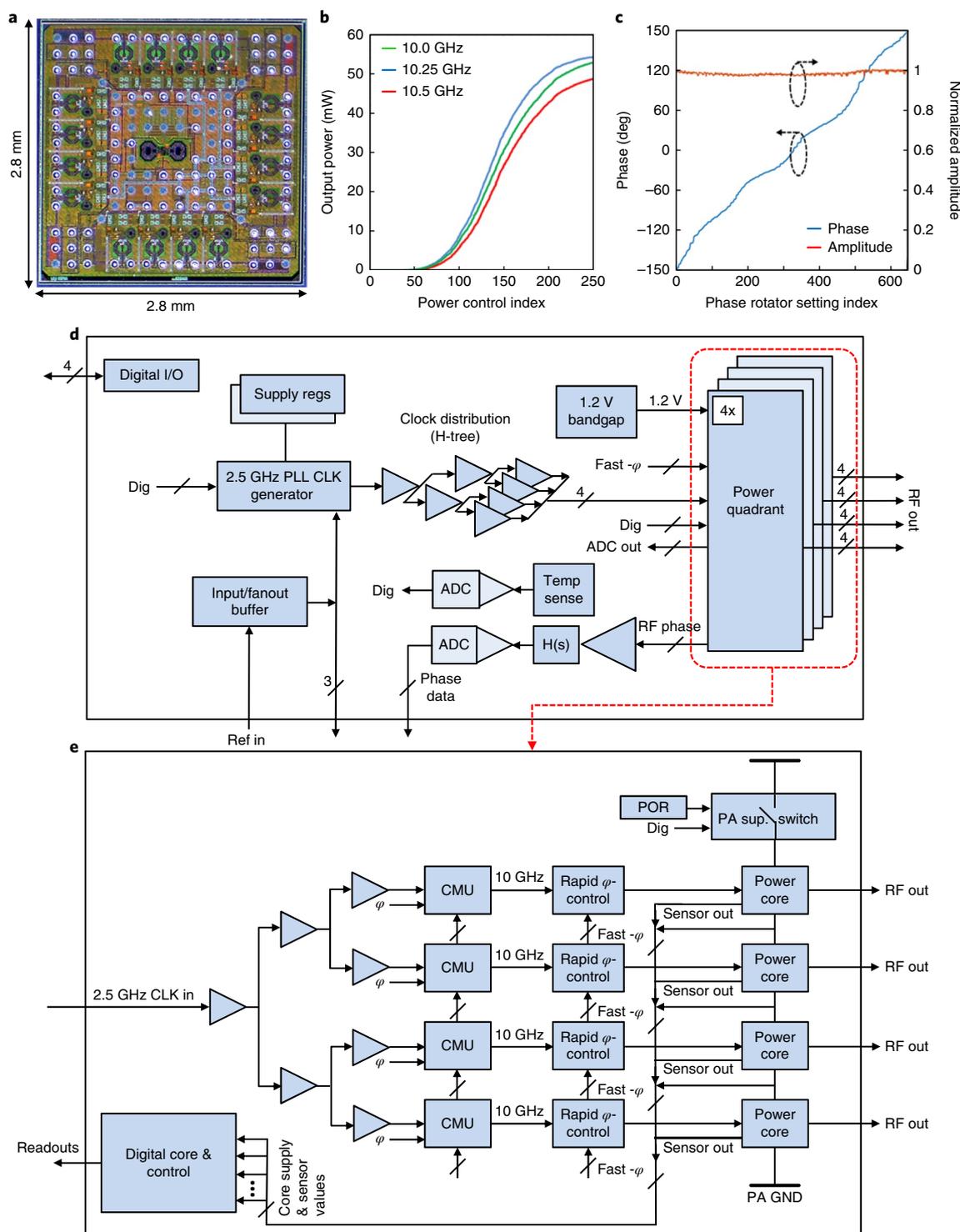


Fig. 4 | Power synthesis and control unit. **a**, Die photograph of the implemented RFIC. **b**, Measured output power as a function of power control index. **c**, Measured phase and amplitude of a PA versus phase rotator setting. **d**, Block diagram of the RFIC architecture. **e**, Block diagram of each power quadrant of the RFIC. CLK, clock; ADC, analog-to-digital converter; I/O, input/output; POR, power-on reset; CMU, clock multiplier unit.

Supplementary Fig. 2). A low-noise, low-frequency 50 MHz clock is distributed across and on each of the scalable array tiles and used as a reference for the frequency synthesizer (phase-locked loop, PLL), as detailed in Supplementary Fig. 1a. To reduce the PLL reference spurs, a loop filter switch similar to ref.⁴⁹ is used with the PLL. The synthesized 2.5 GHz signal is used to further distribute a synchronized reference across the IC to 16 clock multiplier units (CMUs)

with an output frequency of 10 GHz, each followed by a power amplifier (PA) with peak output power of 17 dBm (Fig. 4e). This architecture has several advantages. First, the generation and distribution of a system-level clock is easier and consumes less power at lower frequencies. Second, the use of two frequency synthesizers allows for distribution of a 2.5 GHz reference across the PSCU, which reduces pulling between the channels and lowers the power

consumption. Third, the small multiplier of the CMU stage allows implementation of the phase shift scheme shown in Supplementary Fig. 1b. This is achieved by injecting a constant current into the CMU loop filter, which forces its output to have a phase that is offset compared to the reference. Although such a phase shift scheme affects the spurious tone in the output, the effects are insignificant in our case because the spur is located 2.5 GHz away from the carrier and out of the antenna bandwidth. To enable operation from the larger supply voltages that are more readily available on the tile, the power supplies of the four quadrant PAs are stacked to share the same current while dividing the supply voltage⁵⁰. Sensors within each PA ensure stable voltage sharing among the PAs of the stack, compensate for temperature variations and monitor the system health during operation. This design allows each PA to generate up to 50 mW of output power at 10 GHz with a power-added efficiency (PAE) of 37% (ref. ⁵⁰), which is independent of the output phase set by the CMU (Fig. 4c). A die photograph of the implemented PSCU is shown in Fig. 4a. More details about the power generation mechanism, operation and performance of the PSCU are provided in the Methods.

The tile's multilayer flexible board holds the PSCU (supporting discrete components) and the low-frequency signals and power distribution lines and must serve as part of the radiating structure. The flexible board used in the tile prototype (cross-section in Fig. 3b) has four conductive layers. The top two layers are used for the high-frequency transmission lines, which distribute signal to the radiators and serve as ground for the radiators, while the bottom two layers are used for the PSCU low-frequency reference, signal and power distribution circuitry. This design provides electrical isolation between the radiating elements and the other peripherals, and allows the array to more easily integrate complex structures such as the PV integrated tile presented later in this work.

Tile performance

In addition to radiation metrics such as radiation pattern, beamwidth, steering range and effective isotropic radiated power (EIRP), mechanical metrics such as mass and physical dimensions are essential performance parameters for an FPA system⁵¹. The presented FPA tile consists of 16 FIMP radiators arranged in a 4×4 formation with an 18 mm ($0.6\lambda_0$) spacing, as shown in Fig. 2 (for a detailed configuration schematic see Supplementary Fig. 3). The active area, defined as the fraction of the prototype containing functional elements, is 72×72 mm². The mass of this active area is 5.5 g, corresponding to an areal mass density of slightly more than 0.1 g cm⁻², which is one of the major achievements of the presented foldable and collapsible phased array architecture. Thin carbon fibre frames and a carbon fibre collapsible S-spring⁵² are used to stabilize and separate the FPA's RF and radiator flexible boards to perform phased array characterization.

To best evaluate the impedance matching and mutual coupling between the radiating elements of the FPA tile, the scattering matrix (S parameters) of the FPA is extracted using a finite-element method full-wave electromagnetic solver (ANSYS HFSS). Supplementary Tables 1 and 2 and Supplementary Fig. 4 provide a summary of the extracted S parameters. The resonance frequencies of individual array elements remain within 540 MHz of each other and within 390 MHz of the intended design frequency. All 16 elements are well matched to the intended 75 Ω port impedances, having reflection coefficients (S_{ii}) smaller than -17 dB, which is well below the -10 dB impedance matching criteria. Additionally, the elements are all matched to 75 Ω over the frequency range 9.69–10.86 GHz, which exceeds the range of the PSCU frequency synthesis. The elements of a properly radiating phased array must exhibit low mutual coupling ($S_{ij} < -10$ dB, $i \neq j$) in addition to being well matched. Supplementary Table 2 shows that the designed FPA tile satisfies

both the necessary impedance matching and mutual coupling conditions as $S_{ij} < -11$ dB ($i, j = 1, 2, \dots, 16$) at an operation frequency of 9.8 GHz.

Three representative measurements of beam-steering are presented—broadside ($\varphi = 0^\circ, \theta = 0^\circ$), 30° left ($\varphi = 0^\circ, \theta = 30^\circ$) and 30° up ($\varphi = 90^\circ, \theta = 30^\circ$)—which demonstrate the radiation characteristics and 2D steering capability of the array. (Note that the z axis is normal to the array surface.) For each steering direction, the digitally controlled CMU within the PSCU is programmed with the appropriate phase setting for each of the 16 radiating elements. The complex E field components at a near-field distance are measured using a near-field probe. Figure 5a,b shows the measured x and y components of the E field at a distance of 30 cm at 9.8 GHz for the three selected steering angles. In the presented case where the radiating edges of the array element are oriented along the y axis (Fig. 5f), E_y is the dominant near-field component as the current distribution on the FPA's effective radiating apertures is primarily in the y direction. By performing a near- to far-field transformation, the far-field radiation properties of the FPA tile are obtained. The tile's simulated and measured radiation patterns of the total radiated E field along the E and H planes at $f = 9.8$ GHz are shown in Fig. 5d for the three steering directions. We captured the near- to far-field transformation phenomena through hologram cross-section profiling of the radiated E -field starting from the surface of the FPA tile up to the beginning of the Fraunhofer far-field region (calculated to be 69.1 cm away from the tile). This visualization enables a deeper understanding of the generation and evolution of the radiated field. The holograms of the measured radiated field profiles are plotted every 10 cm along the direction of propagation for the three beam-steering scenarios. The field evolution of the FPA tile for ($\varphi = 0^\circ, \theta = 30^\circ$) is demonstrated in Fig. 5c (similar hologram plots for ($\varphi = 0^\circ, \theta = 0^\circ$) and ($\varphi = 90^\circ, \theta = 30^\circ$) steering angles are provided in Supplementary Fig. 5).

To steer the beam by 30° in elevation or azimuth, a 108.8° linear progressive phase shift between adjacent radiators (in the x or y directions, respectively) is required in a phased array with element spacing of 0.6λ . However, in the presented FPA, the drive phases of the FPA elements also account for the phase shift introduced by the difference in the transmission line lengths connecting the PA outputs to the corresponding radiating element. The drive phase information for each array element used to steer the beam towards the three chosen directions is provided in Supplementary Table 3. The measured and simulated radiation pattern comparison of the E_θ and E_φ far-field components shown in Supplementary Fig. 6 demonstrates excellent agreement for all three beam-steering scenarios. The agreement between the predicted and measured radiation characteristics extends beyond just the radiation pattern shape and also includes the half-power beamwidth, radiation efficiency and sidelobe levels, as is evident from Supplementary Table 4. In the presented prototype FPA tile, classical phased array theory predicts that the radiation main beam can be steered $\pm 56.4^\circ$ before a grating lobe starts to appear⁴³. The maximum radiated power was obtained with 12 elements turned on. The radiation characteristic summary of the phased array when 12 elements are turned on is provided in Supplementary Table 5 and Supplementary Figs. 7–9. The measured EIRP of the FPA over the frequency range 9.4–10.4 GHz for the FPA is shown in Fig. 5e when the four corner array elements are turned off. This mode of operation is enabled by independent control over each transmitter on the PSCU. A nearly constant maximum EIRP of +38.2 dBm is achieved at 9.56–9.72 GHz. At 9.8 GHz the phased array offers an EIRP of +37.1 dBm with a total radiated power of +19.2 dBm. Thus, the presented FPA tile architecture is capable of generating a high-power microwave beam with full control over the beam shape and direction while being ultra-lightweight and compact.

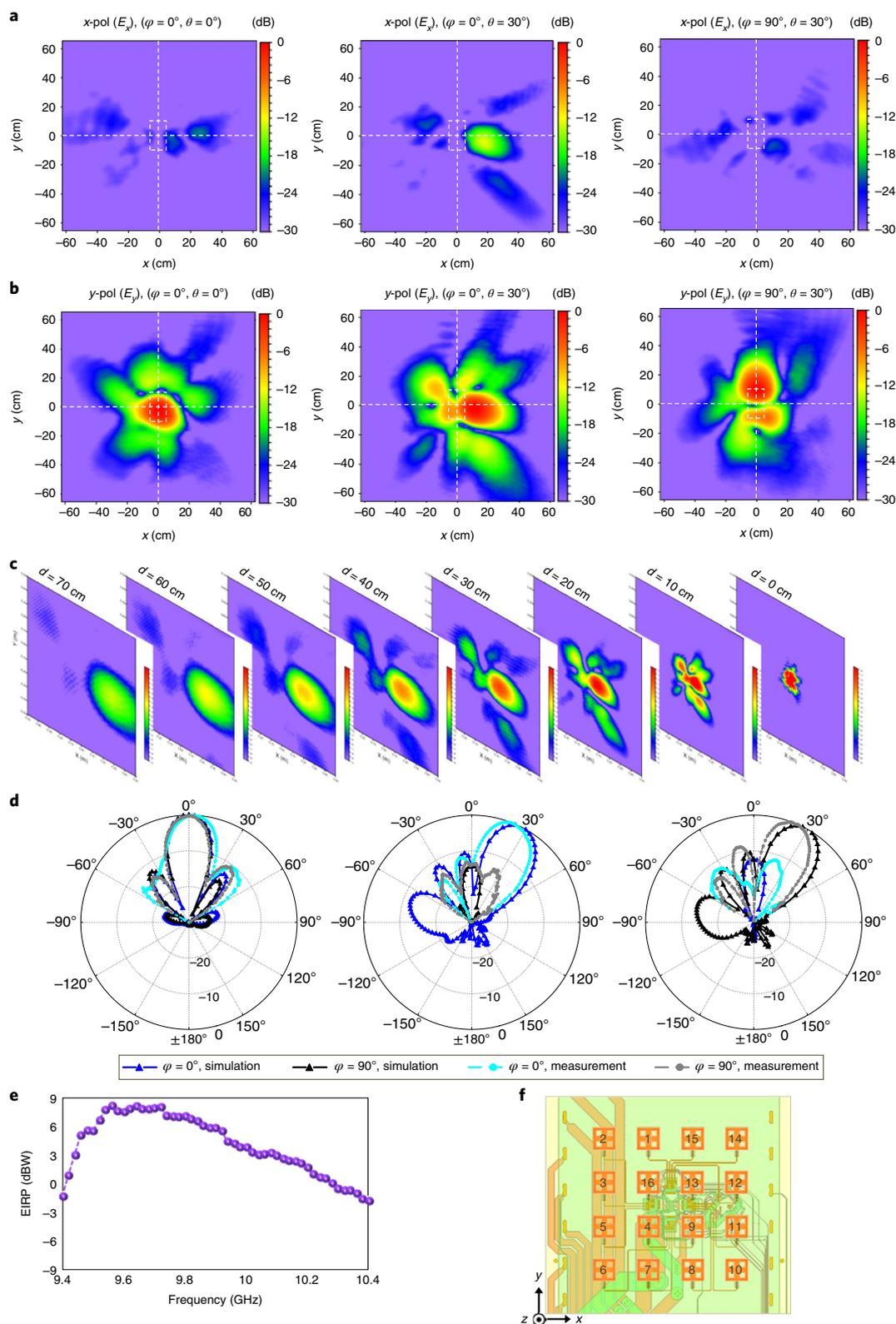


Fig. 5 | Performance of the 4×4 FPA system prototype. **a**, Measured near-field cross-polarization component of the E field (E_x). **b**, Measured near-field co-polarization component of the E field (E_y) for three scan angles, $(\varphi = 0^\circ, \theta = 0^\circ)$, $(\varphi = 0^\circ, \theta = 30^\circ)$ and $(\varphi = 90^\circ, \theta = 30^\circ)$, shown from left to right. **c**, Measured hologram plots over different x - y plane cross-sections along the z direction (propagation direction) for every 10 cm of propagation for scan angle $(\varphi = 0^\circ, \theta = 30^\circ)$. **d**, Simulated and measured radiation patterns of the total radiated E fields along the E plane ($\varphi = 90^\circ$) and H plane ($\varphi = 0^\circ$) for three scan angles, $(\varphi = 0^\circ, \theta = 0^\circ)$, $(\varphi = 0^\circ, \theta = 30^\circ)$ and $(\varphi = 90^\circ, \theta = 30^\circ)$, shown from left to right. **e**, Measured EIRP. **f**, Radiating element referencing. The near-fields, far-fields and hologram plots are measured at $f = 9.8$ GHz. Each PA draws nearly 180 mA at 1.1 V.

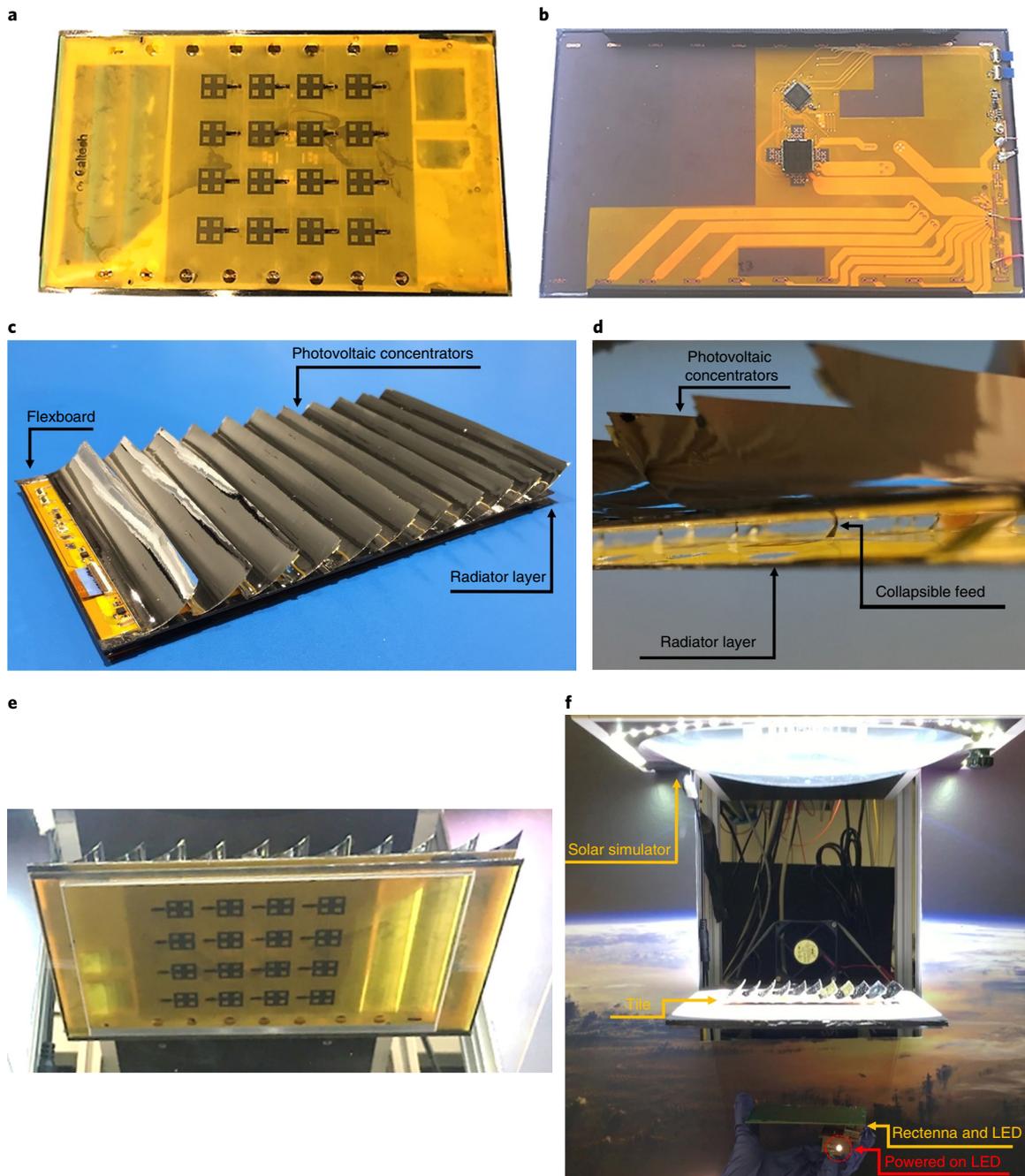


Fig. 6 | Photographs of a 4×4 FPA tile integrated with PV solar cells and concentrators. **a**, View of the radiator side of the tile. **b**, View of the RFIC side of the tile. **c**, PV concentrators of the integrated tile. Concentrators are mounted on the same side of the four-layer RF flexible board as the RFIC. **d**, Side view of the integrated tile. RF feedlines and the antenna layer are isolated from the photovoltaics and concentrators. Collapsibility is maintained in the integrated tile. **e**, Radiator side of the integrated tile. **f**, Demonstration of power collection and transmission. A solar simulator illuminates the tile, which radiates RF power to the rectenna, lighting an LED.

PV powered tile

Co-located photovoltaics and RF antenna apertures are attractive for many applications because both the collected solar power and the antenna gain are proportional to the shared aperture area. Optically transparent antennas^{53,54} and partially shared apertures⁵⁵ have been proposed for collecting solar power and radiating RF power from the same side of a single aperture, which leads to a reduction of the effective aperture for both PV and RF subsystems. Alternatively, collecting solar power from one side of an aperture and reflecting RF from a passive reflectenna on the other side has been demon-

strated in ref.⁵⁶ as a way to achieve full aperture utilization for both subsystems. This work demonstrates a shared PV–RF aperture with electronic beam-steering, without a fundamental aperture loss. The RF tile is combined with a concentrator-based PV array, demonstrating a self-contained power transfer system. The concentrator-based solar power generation used in our architecture is similar to the system found in refs.^{57,58}. The radiator side and the PSCU side of the tile are shown in Fig. 6a,b, respectively. The combined PV tile is intended for use in a large-scale space solar power transfer array but could also be used as a self-powered terrestrial RF beacon. PV

power is well suited for this scalable tile architecture because each tile features self-contained power collection and transmission. The distributed power transfer architecture avoids high-mass d.c. power lines within the array and is robust to failure of individual photovoltaics, integrated circuits or radiators. The solar cell design uses concentrator blinds mounted on the PSCU side of the multilayer flexible board, as shown in Fig. 6c. Thin carbon fibre concentrator blinds are a low-mass alternative to conventional flat-panel solar cells. Each blind concentrates incident light onto a small strip of PV material mounted across the back of the blind directly in front of it. The concentrator and PV design are described in refs. 57,58. Electrical and physical integration of the photovoltaics and concentrators occur only on the PSCU side of the flexible board. This maintains the collapsibility of the air gap and feeds shown in Fig. 6d and does not change the radiation characteristics of the antennas as the flexible board ground layer provides shielding. Figure 6e shows the unmodified radiators on the bottom side of the tile. Figure 6f shows the tile illuminated by an AM0 solar simulator (simulating the sunlight spectrum outside the Earth's atmosphere), demonstrating solar power collection and RF wireless power transfer to illuminate a light-emitting diode (LED) on a handheld rectenna board.

Conclusions

We have reported a flexible integrated circuit-based phased array architecture that is scalable, lightweight and can be stored compactly. To demonstrate the capabilities of the array architecture, we have built a 16-element 4×4 FPA tile operating at 9.4–10.4 GHz. This tile was also combined with a concentrator-based solar cell to create a self-contained power collection and transfer unit. The FPA architecture could be used in a variety of applications, including large-scale deployable arrays for spacecraft and small wearables.

Methods

RF design specification. The presented proof-of-concept tile was designed to have a nominal operational frequency 9.8–10 GHz and impedance of 75Ω . The radiators and their feedline were fabricated on a $25.4\text{-}\mu\text{m}$ -thick polyimide-based (Pyrulux-AP8545R, $\epsilon_r = 3.5$, $\tan \delta = 0.02$) single layer. A $17.8\text{-}\mu\text{m}$ -thick copper layer was used to form the metal patterns. The RF flexible board was a four-layer board made of two identical dual-layer conductor/polyimide/conductor sheets, each consisting of a $101.8\text{-}\mu\text{m}$ -thick Pyrulux-AP8545R flexible substrate sandwiched between two $17.8\text{-}\mu\text{m}$ -thick copper layers. These two dual-layer flexible printed circuit boards were bonded together using a $50.8\text{-}\mu\text{m}$ -thick adhesive layer ($\epsilon_r = 3.5$, $\tan \delta = 0.02$). A cross-sectional view of the radiator layer and the RF four-layer flexible boards is shown in Fig. 3b. Based on the described RF flexible board stack, a $99\text{-}\mu\text{m}$ -wide microstrip transmission-line will have a 75Ω characteristic impedance at 10 GHz (verification is provided in Fig. 3d, where the shown Smith chart indicates a $75.01 + j1.48 \Omega$ characteristic impedance at 10 GHz.) At 10 GHz, a via transition with a radius of $152.4 \mu\text{m}$, via cap radius of $558.8 \mu\text{m}$ and via hole radius of $965.2 \mu\text{m}$ will provide a 75Ω RF transition.

The FIMP radiators consisted of an edge-fed $9 \times 9 \text{ mm}^2$ square metallic patch with a 3 mm gap ($\sim \lambda_0/10$ at $f = 10 \text{ GHz}$, considering the single-layer flexible board thickness is much smaller than the air gap) between the patch and ground plane. Four $2.3 \times 2.3 \text{ mm}^2$ square cuts were made in the patch, as shown in Fig. 3a. The feed transition included an interdigital capacitor connected to a tapered section. The configuration and design layout of the interdigital capacitor used for the impedance matching, loading and size reduction of the FIMP antenna are shown in Supplementary Fig. 18a. The interdigital capacitor consisted of four identical fingers, all with length and width of 1.1 mm and 0.1 mm, respectively, and a 0.1 mm gap distance between every two consecutive fingers. The impedance of the discussed interdigital capacitor was extracted using a full-wave simulation using ANSYS HFSS. The extracted normalized impedance of the interdigital capacitor is shown in Supplementary Fig. 18b. At 10 GHz the interdigital capacitor had an impedance value of $0.4425 - j144.5475 \Omega$ and an extracted total capacitance value of 0.108 pF . The taper section had a length of 1.84 mm connecting the interdigital capacitors to a 1.5-mm-long copper trace with a width of $99 \mu\text{m}$. These small $99\text{-}\mu\text{m}$ -wide traces of the feedlines were designed to overlap and be aligned with the corresponding 75Ω transmission-lines on the top side of the RF multilayer flexible board. Cuts were made around the free boundaries for each antenna feedline transition, which were released. These feedlines were then attached to the 75Ω transmission-lines on RF flexible board using low-temperature solder paste, resulting in the desirable flexible and collapsible ‘ f ’-shaped feeding transition. To determine the optimum size of the square cut inserted in the patch with minimum impact on the radiator's performance, a comprehensive analysis was carried out.

This analysis was performed in terms of the resonance frequency, impedance matching, antenna gain, antenna efficiency and radiated power as a function of cutout width using ANSYS HFSS. A summary of the analysis is provided in Supplementary Fig. 10. The results indicate that the performance of the radiator remains almost constant when the width of the square cutouts is increased up to 2.3 mm. However, beyond 2.3 mm the performance of the FIMP radiator is drastically affected and degraded. Thus, considering all the tradeoffs between the antenna performance parameters and the size of the inserted square cuts, the optimum squares should have a width of 2.3 mm, resulting in a 26.1% patch area copper removal.

RF power generation. The PSCU, consisting of a $2.8 \times 2.8 \text{ mm}^2$ chip, was flipped onto an $11 \times 11 \times 0.5 \text{ mm}^3$ RO4003 interposer. The chip and interposer had a combined mass of 230 mg and were mounted on the tile's flexible board, opposite the FIMP radiator side. The tile was highly flexible and could be rolled, flexed or twisted (Fig. 2). As an example, the tile was rolled into a cylinder of radius 3 cm and unfolded to its planar form without damaging the tile's structural integrity, its electric connections or interposer mounting (Fig. 2d).

The required output 10 GHz signal was synthesized on-chip in two steps. First, a central PLL unit generated a 2.5 GHz signal to be distributed across the chip to each of the 16 channels. A CMU with a multiplication factor of four generated the local 10 GHz signal, which was fed into each of the PAs. The CMU also performed the phase shift. To operate at higher than the nominal transistor voltage of 1 V, the PAs were stacked in groups of four, sharing their supply current and dividing the supply voltage. This is in contrast to the previously demonstrated cascode and stack transistor techniques used to reduce the voltage stress on any single transistor^{59,60}. The block diagram of the power quadrant architecture is shown in Fig. 4d,e. A digital feedback control loop sensed the current and voltage swing on each of the PA cores and changed the individual power supplies in response to maintain desired stable operation (Fig. 4d). For this reason, d.c. current sensors and cascode peak voltage sensors were implemented in the output stage of each PA, as well as within the PA cores. The power supply state was digitized and assessed using on-chip, eight-bit successive approximation register (SAR) ADCs and an off-chip microcontroller (ARM Cortex-M0), which communicated through a serial interface.

FPA tile EIRP measurement. To measure the EIRP of the FPA tile, a standard gain WR-90 horn antenna with a known gain was used as a receiver. The horn antenna was then connected to a power meter providing the received power information while the FPA system was placed at a far-field distance from the horn antenna and used as a transmitting antenna. By using the Friis equation⁴³, the EIRP of the FPA was then calculated.

Hologram measurement and plots. The hologram plots were generated using the NSI2000 near-field/far-field measurement range software.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

Code availability

High-level description of the code created to drive the hardware is available from the corresponding author upon reasonable request.

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Author contributions

A.H. conceived the idea of the flexible RF phased array. M.R.M.H., A.C.F., M.G.-K. and A.H. designed the flexible array and its electromagnetic components. M.R.M.H., A.C.F., M.G.-K., F.B., B.A. and A.S. performed the reported measurements of the system. B.A., F.B., M.G.-K., A.S. and A.H. designed and implemented the integrated circuit. M.D.K., E.L.W., P.E., N.V., E.E.G., C.L., F.R., S.P. and H.A.A. contributed to the design and implementation of the PV concentrators and cells. M.R.M.H., A.C.F., A.H. and M.G.-K. prepared the manuscript.

Competing interests

A.H., B.A. and F.B. are co-founders and shareholders of Auspion Inc., which is involved in wireless power transfer applications. A.S. is currently employed at Auspion Inc. Several

patent applications that cover certain aspects of the design of the integrated circuit and flexible substrate have been filed.

Additional information

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